

# SCREME: A Scalable Framework for Resilient Memory Design

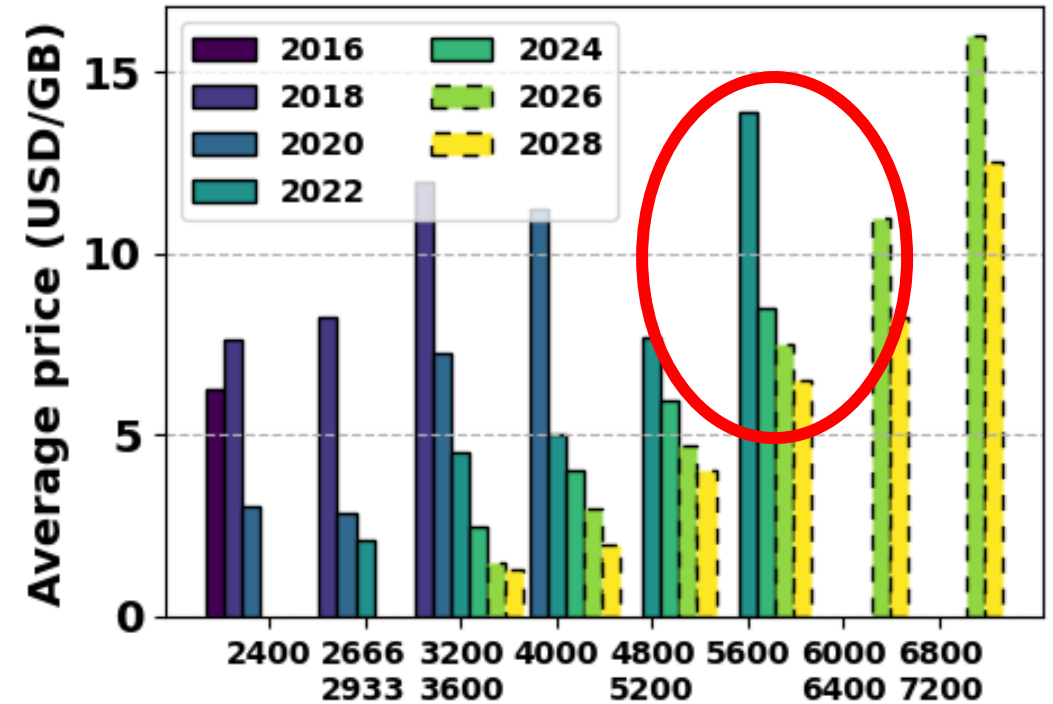
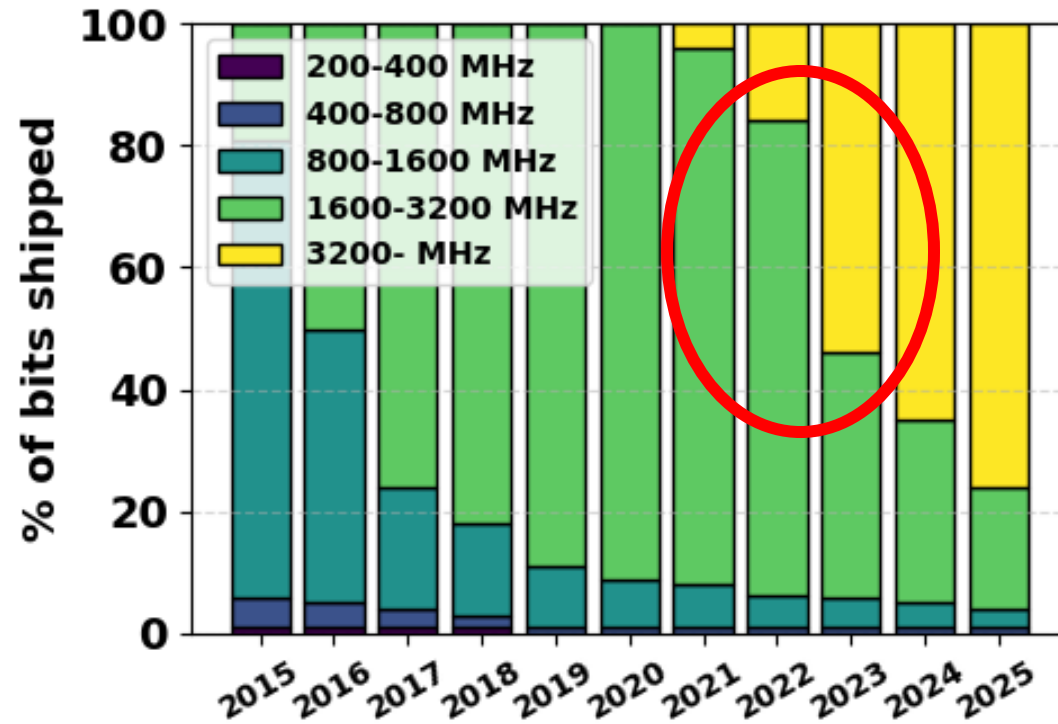
*Fan Li<sup>†</sup>, Mimi Xie<sup>‡</sup>, Yanan Guo<sup>\$</sup>, Huize Li<sup>†</sup>, Xin Xin<sup>†</sup>*

†University of Central Florida, USA

‡ University of Texas at San Antonio, USA

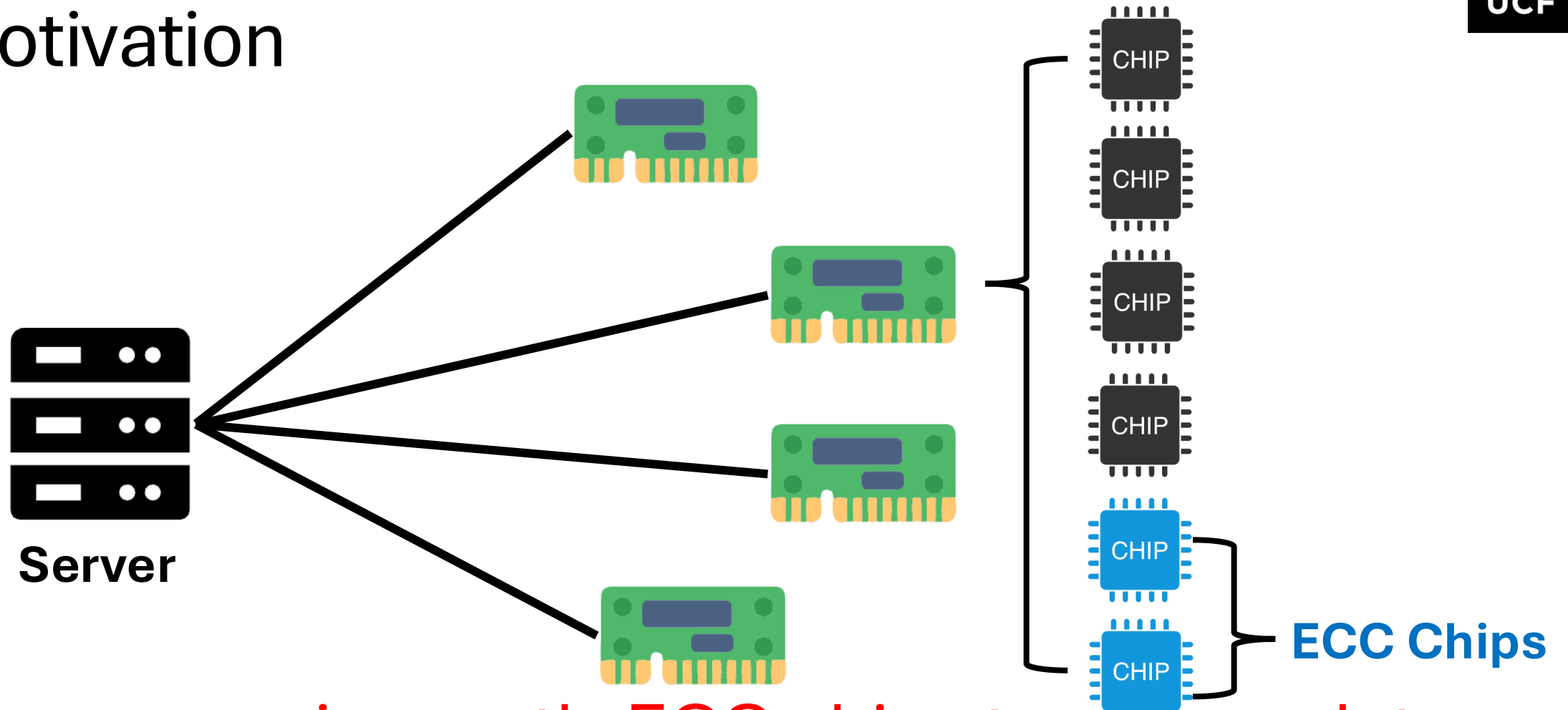
\$ University of Rochester, USA

# Motivation



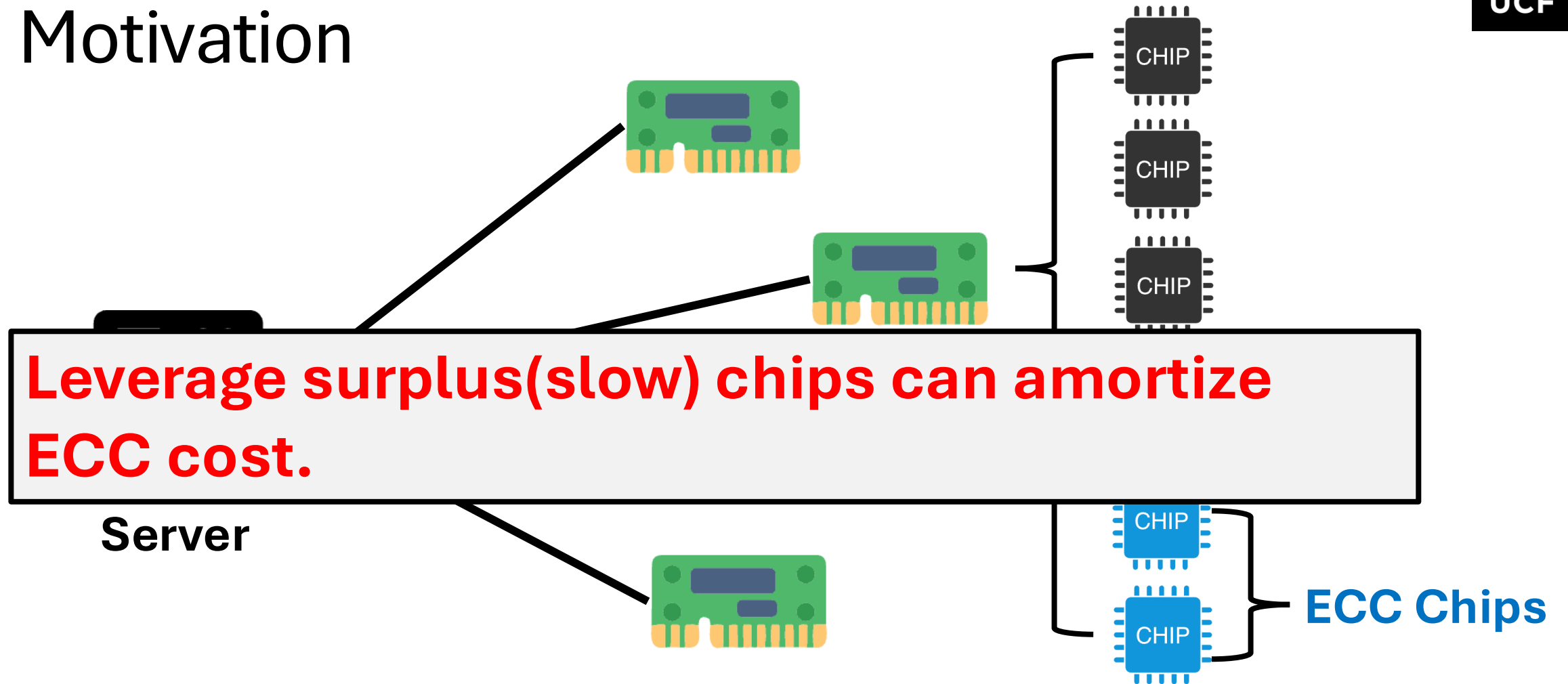
Legacy DRAM chips are **slow** but **low-cost**.

# Motivation



Servers require costly ECC chips to ensure data-integrity.

# Motivation

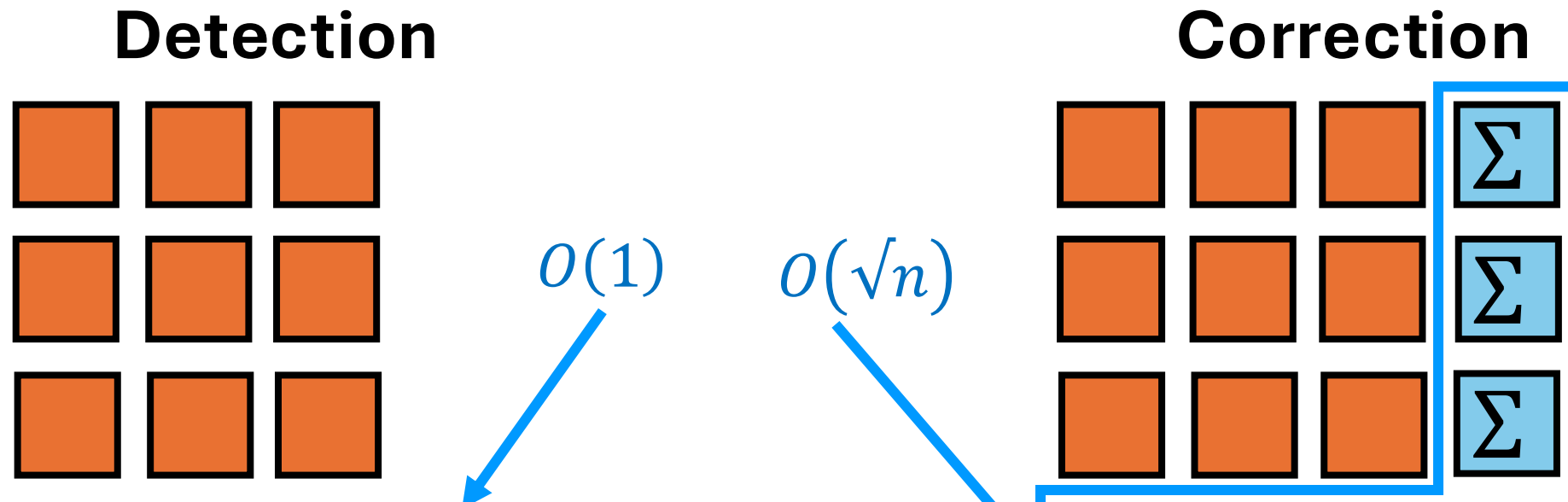


**Leverage surplus (slow) chips can amortize ECC cost.**

Server

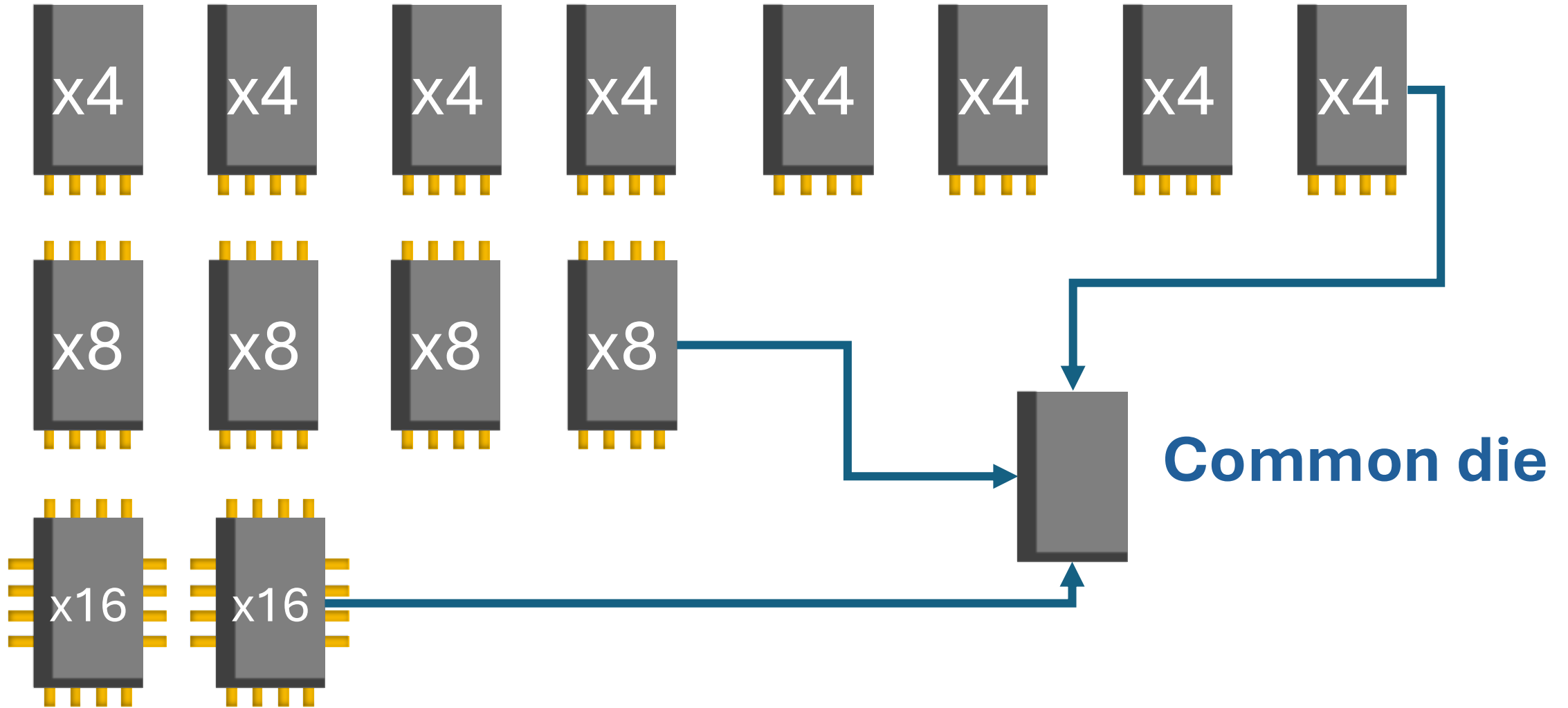
ECC Chips

# Foundation1: Detection is much light-weight than correction

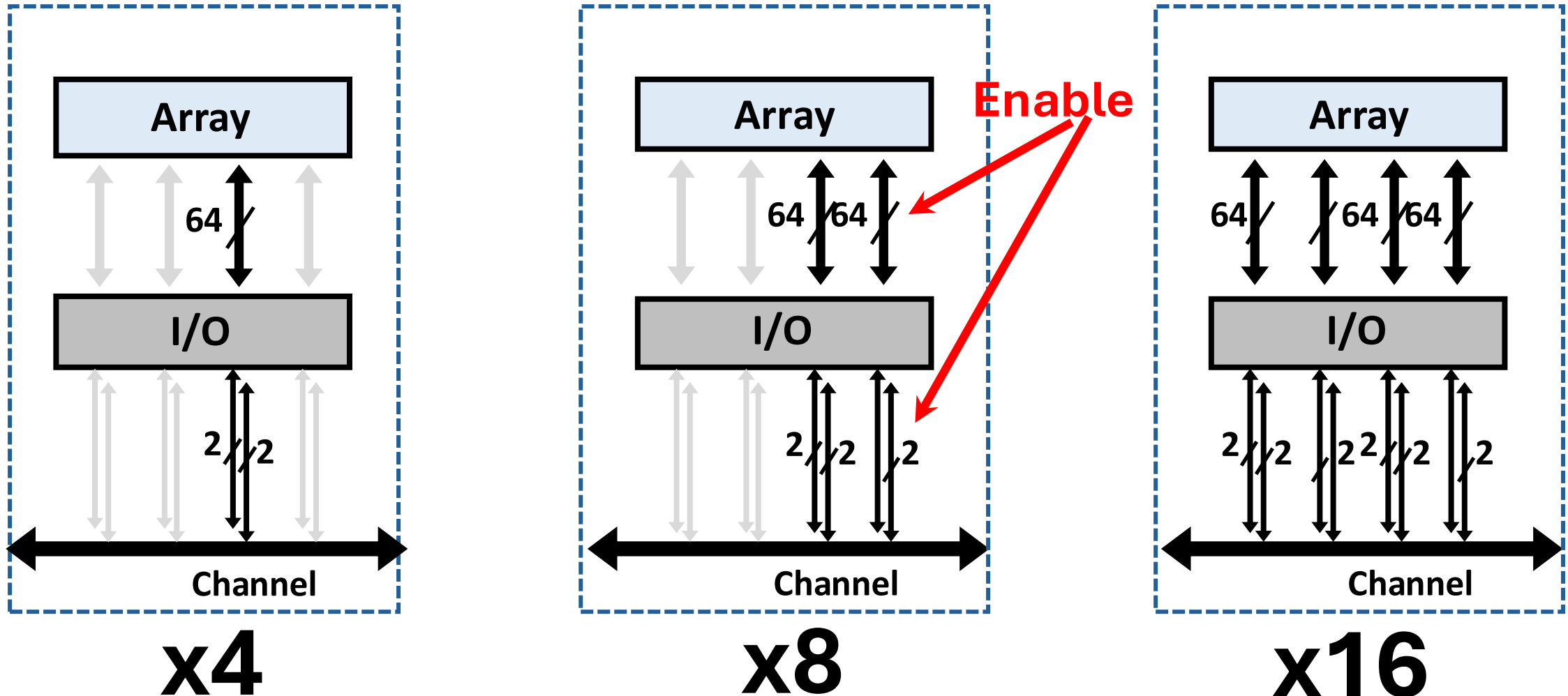


**Detection** is much more **light-weight** than **correction**

# Foundation2: Chips share the same package

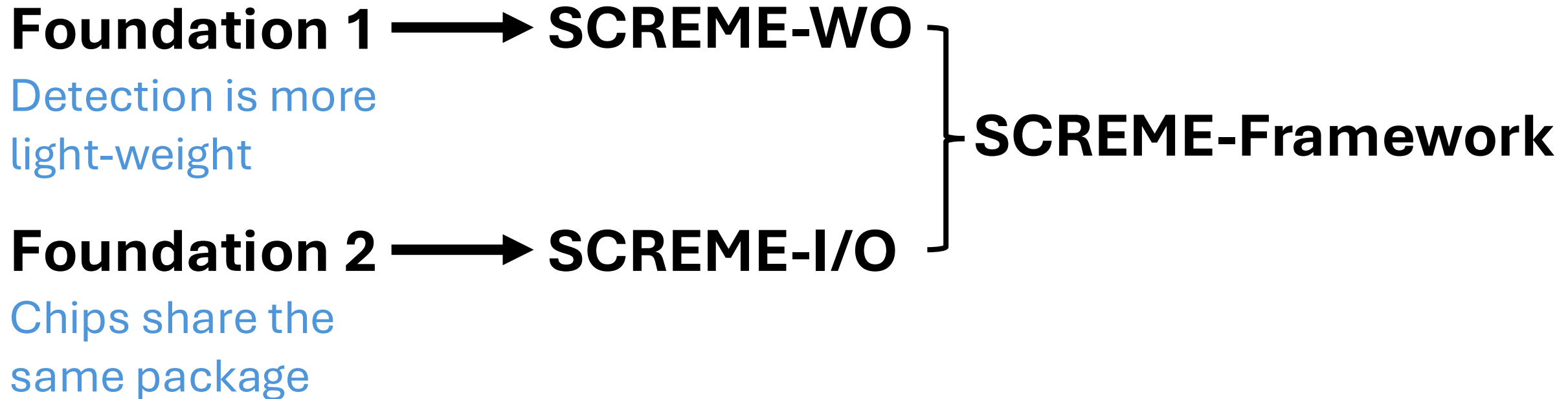


# Foundation2: Chips share the same package



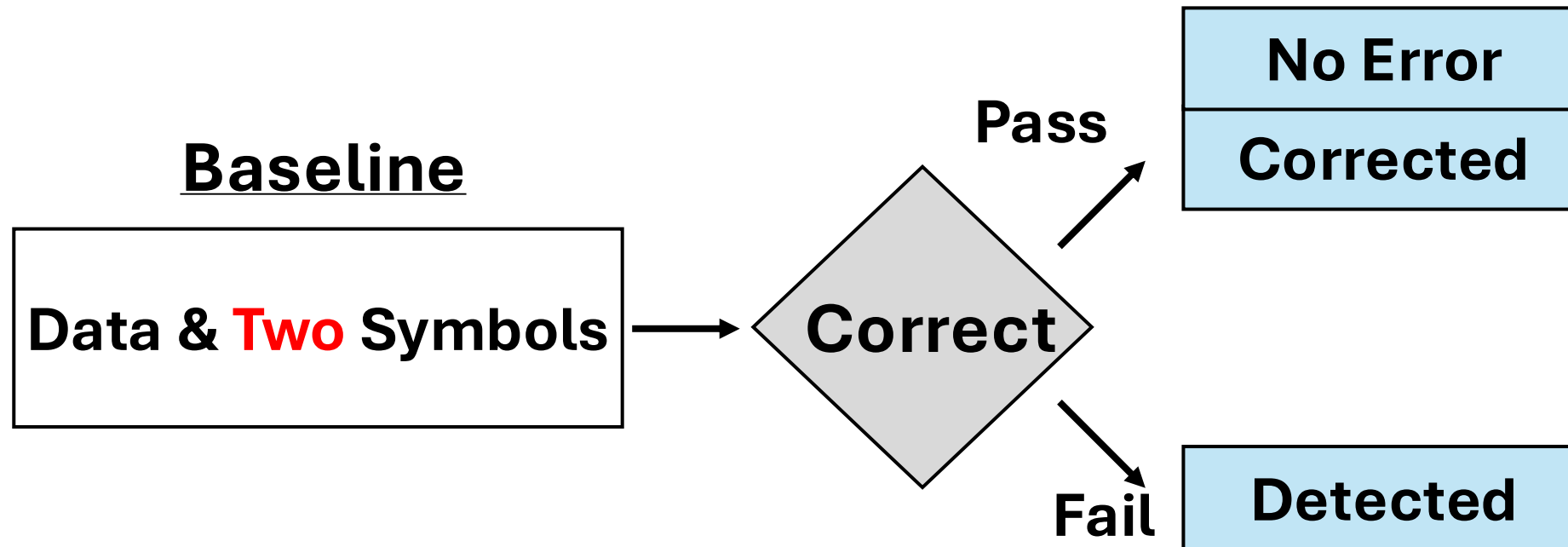
# SCREME-Framework

- **Objective:** Enable scalable and cost-efficient memory fault tolerance framework.



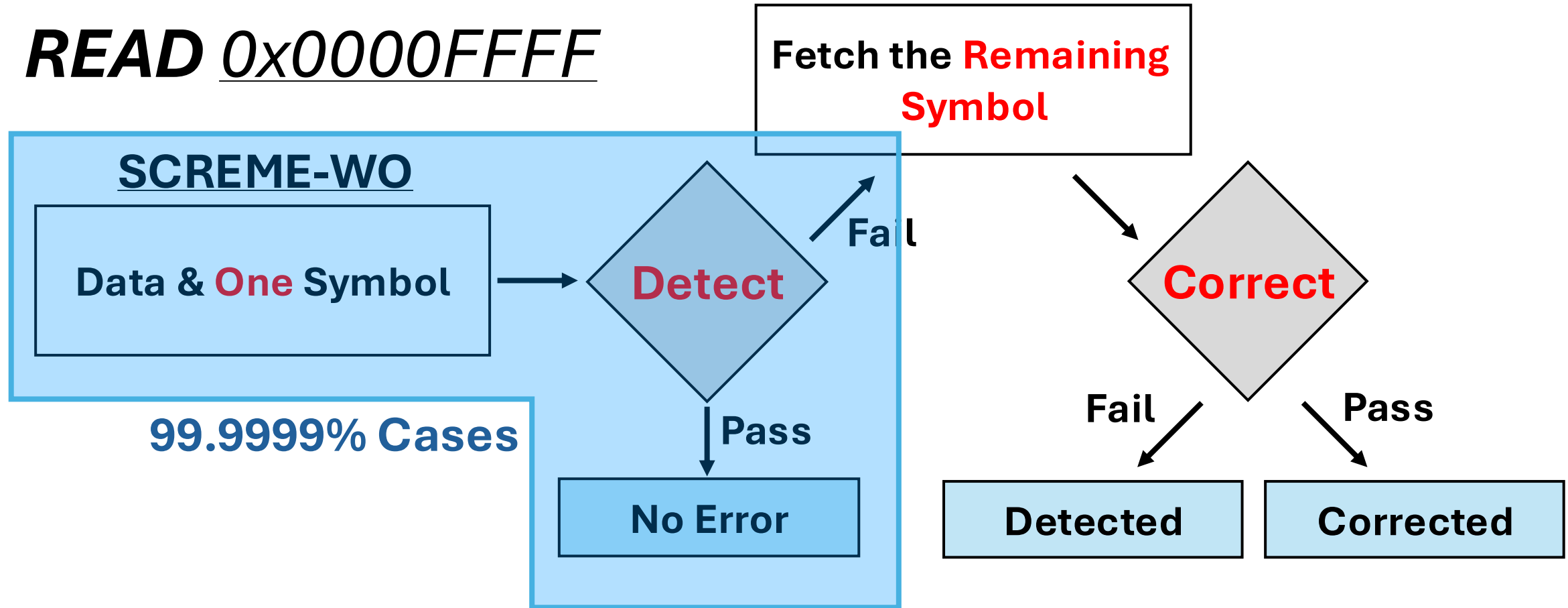
# Design1: SCREME-WO(Write-Only ECC)

***READ 0x0000FFFF***



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***READ*** 0x0000FFFF



# Design1: SCREME-WO(Write-Only ECC)

Legacy chips are **slow** but **low-cost**

*READ*: **Half** ECC bandwidth(fetch **one** symbol)

*WRITE*: **Full** ECC bandwidth(update **all** ECC symbols)

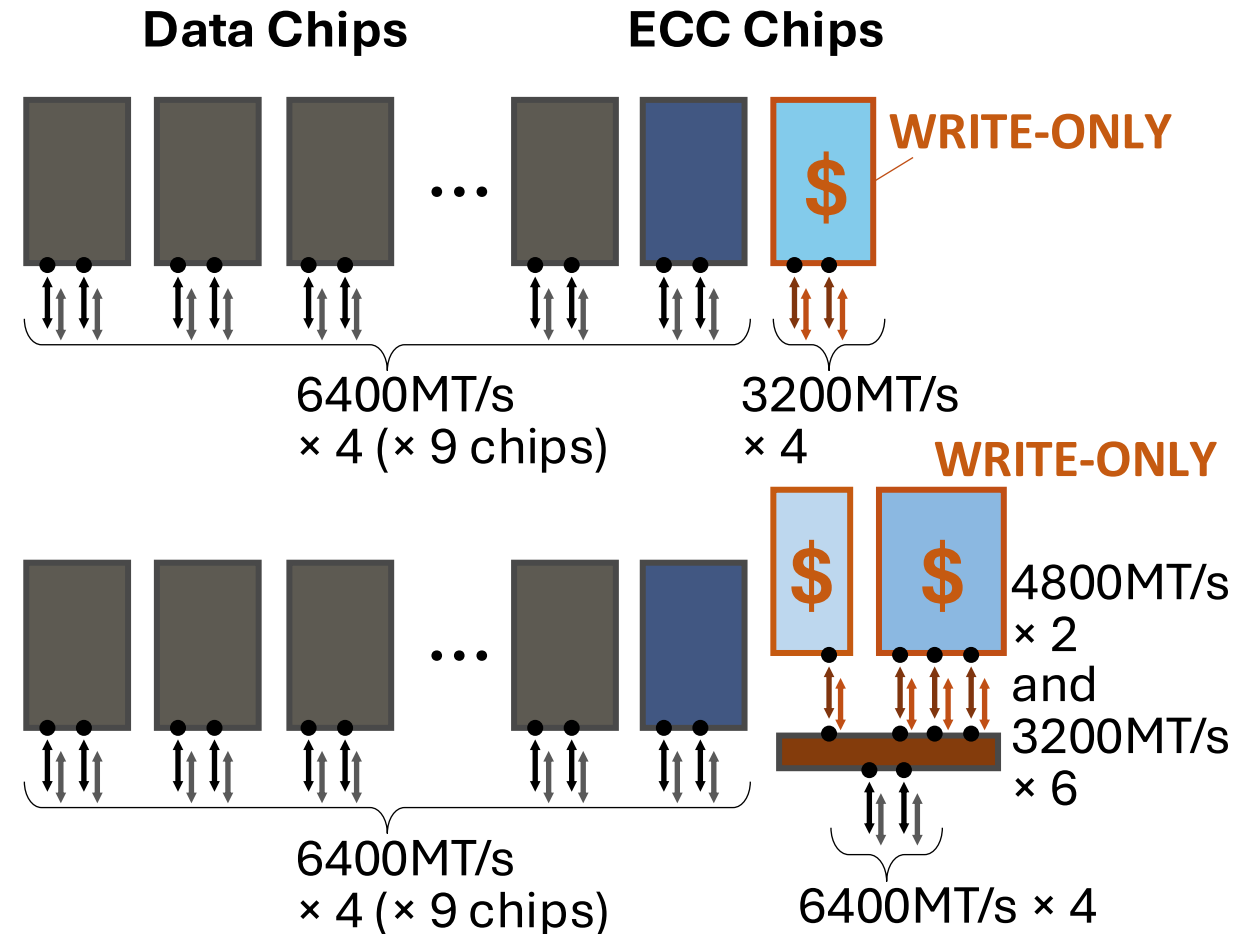
Repurpose ECC bandwidth:

*From READ to low-cost chip's SLOW WRITE*

# Design1: SCREME-WO(Write-Only ECC)

Employ a slow chip as a **write-only ECC chip**.

Employ **various slow chips** to store parity data with buffer support.



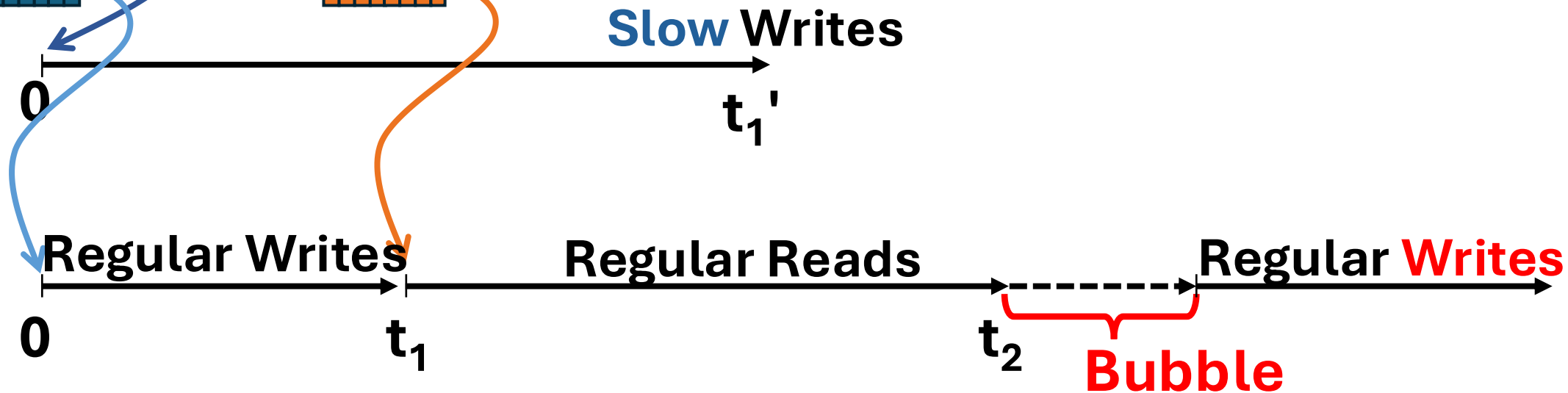
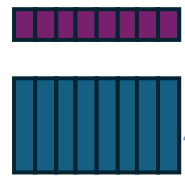
# Design1: SCREME-WO(Write-Only ECC)

**Bubble condition:  $t_1' - t_1 > t_2$**

Parity Data Buffer

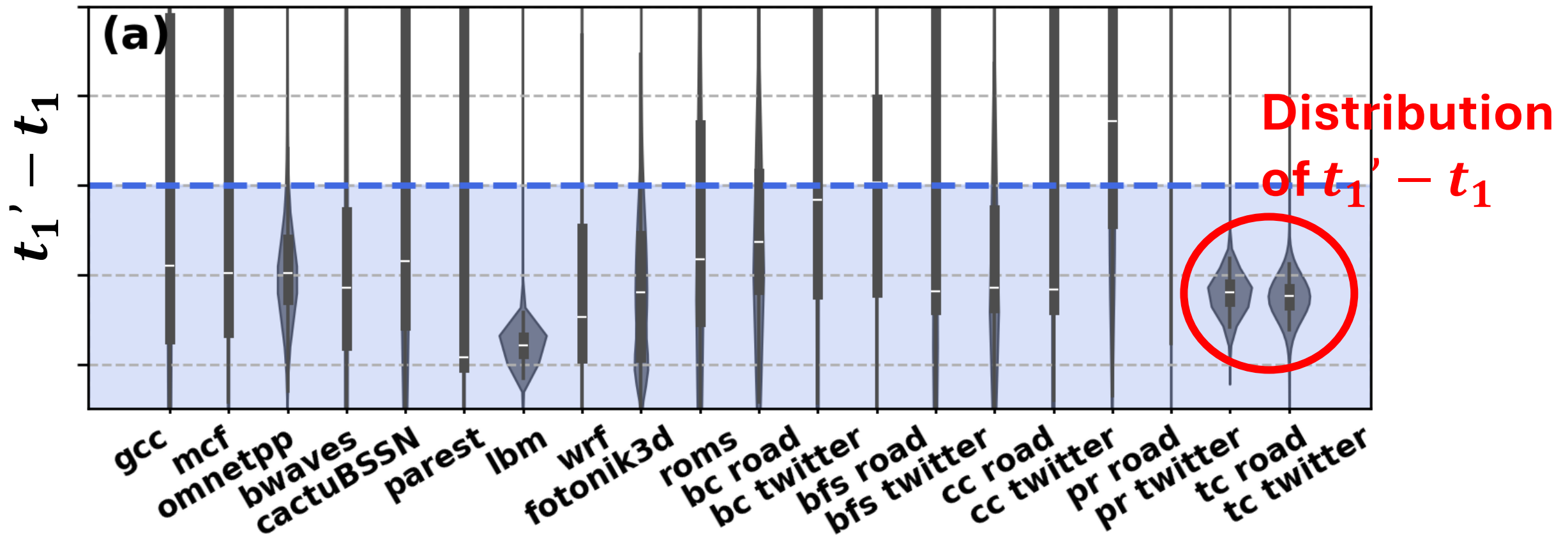
Write Buffer

Read Buffer



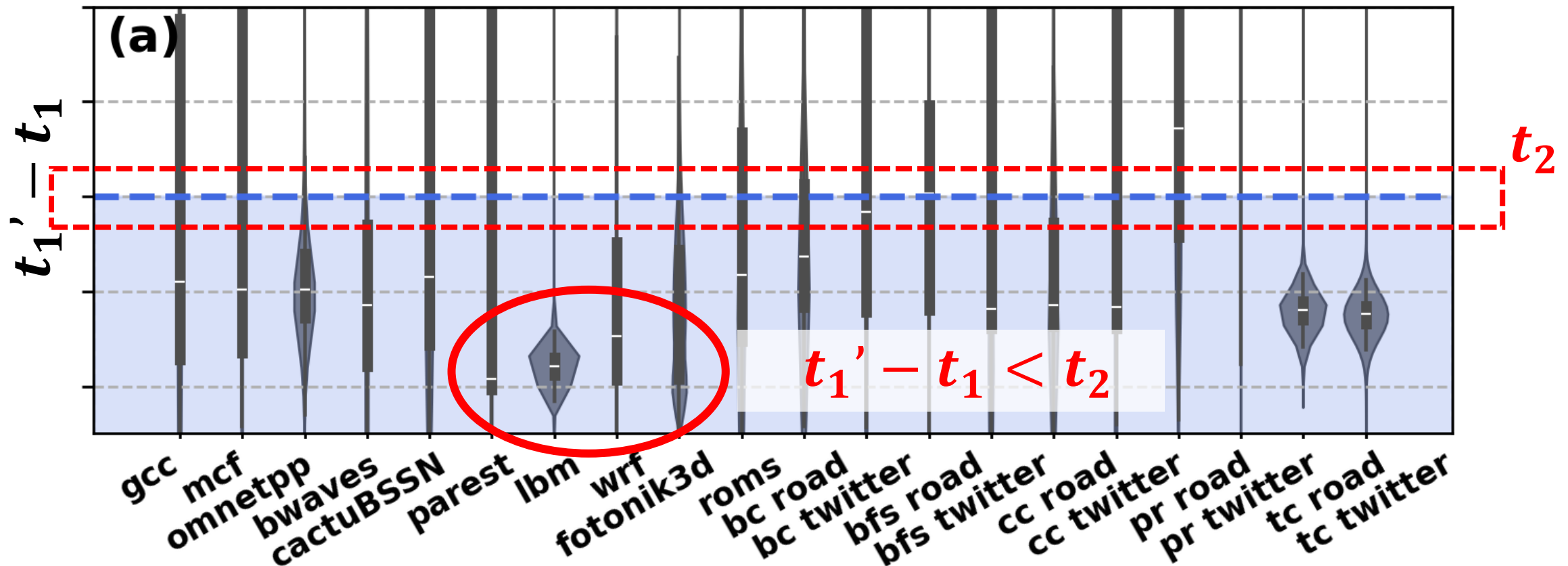
# Design1: SCREME-WO(Write-Only ECC)

Regular: 6400MHz & Slow: 1600MHz



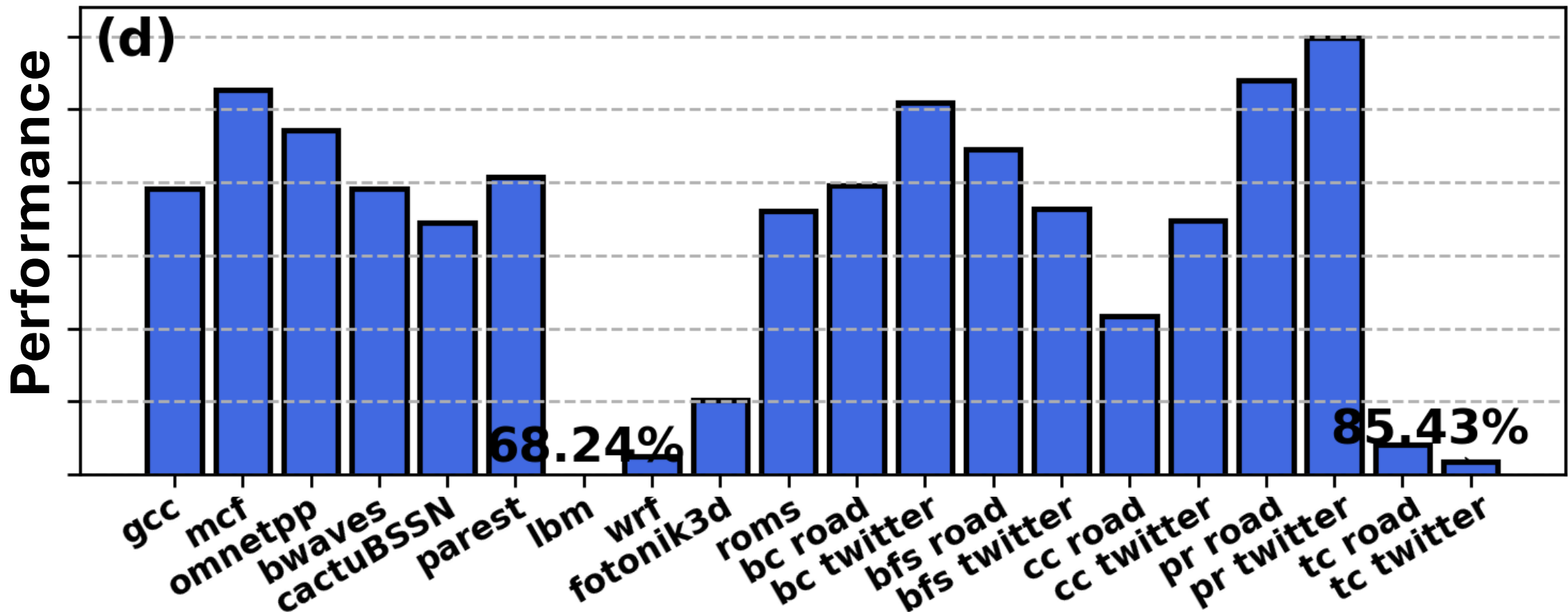
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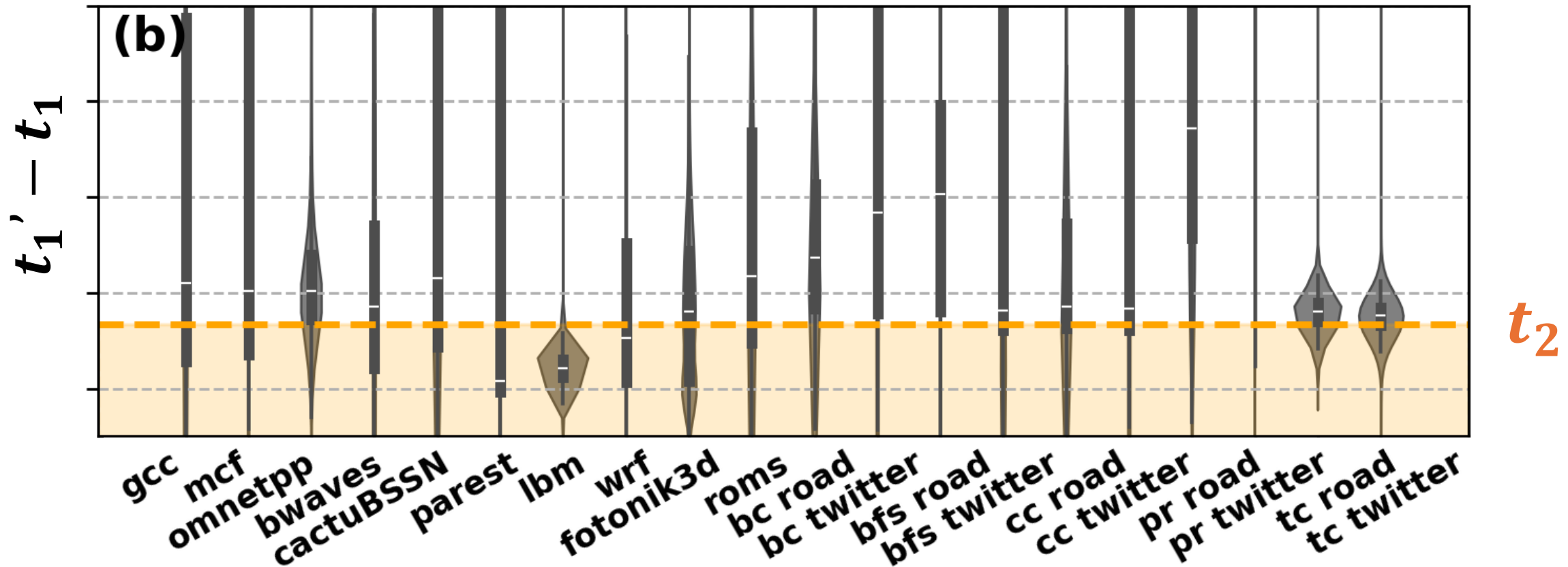
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Regular: **6400MHz** & Slow: **1600MHz**



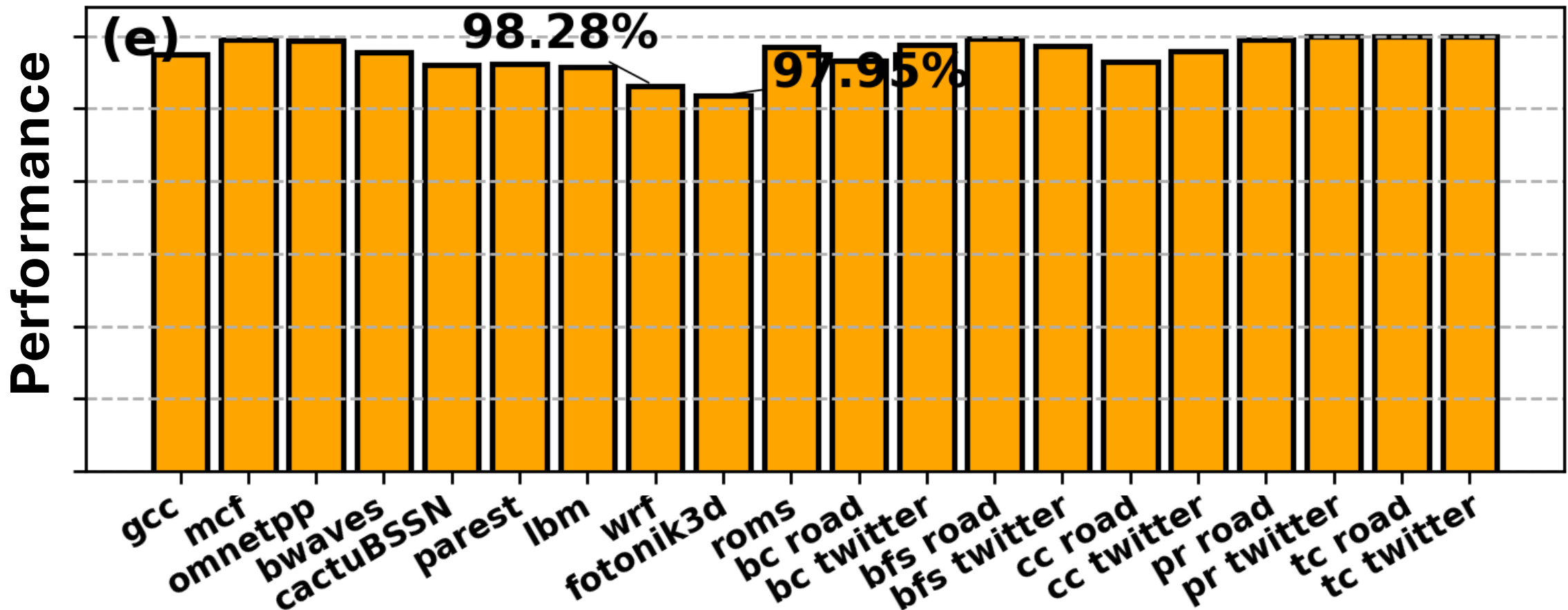
# Design1: SCREME-WO(Write-Only ECC)

Regular: 6400MHz & Slow: 2400MHz



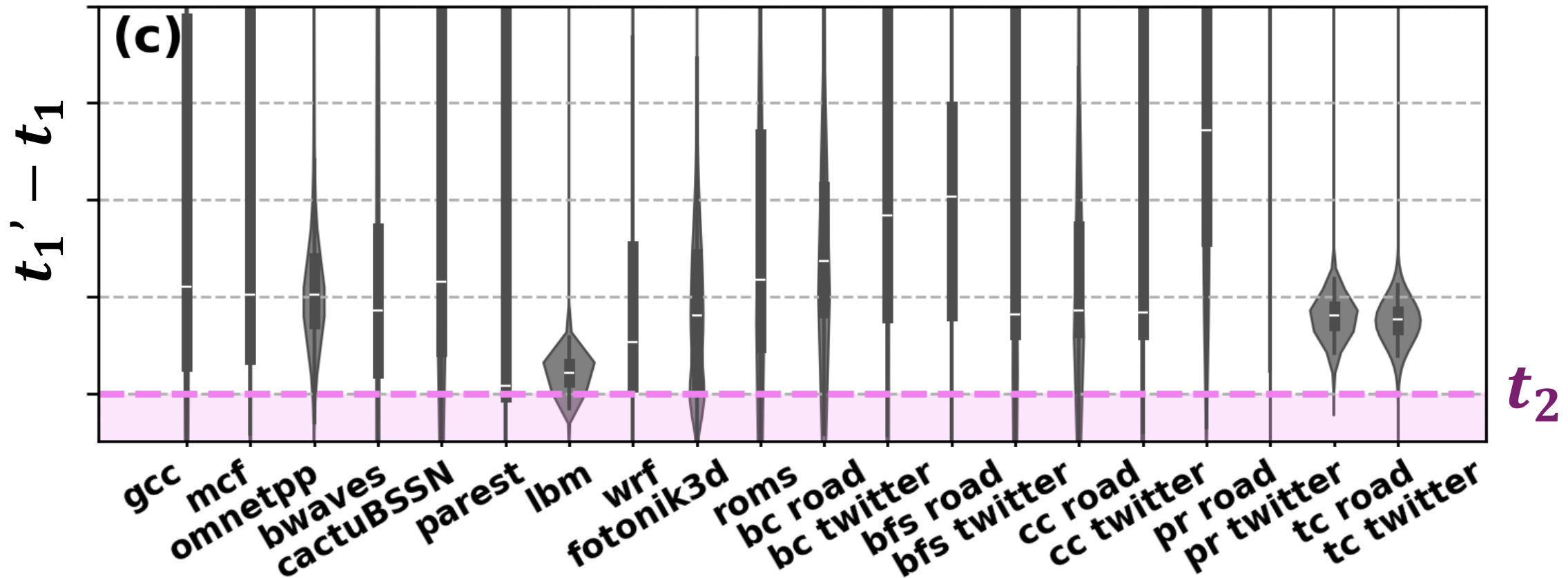
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Regular: 6400MHz & Slow: 2400MHz



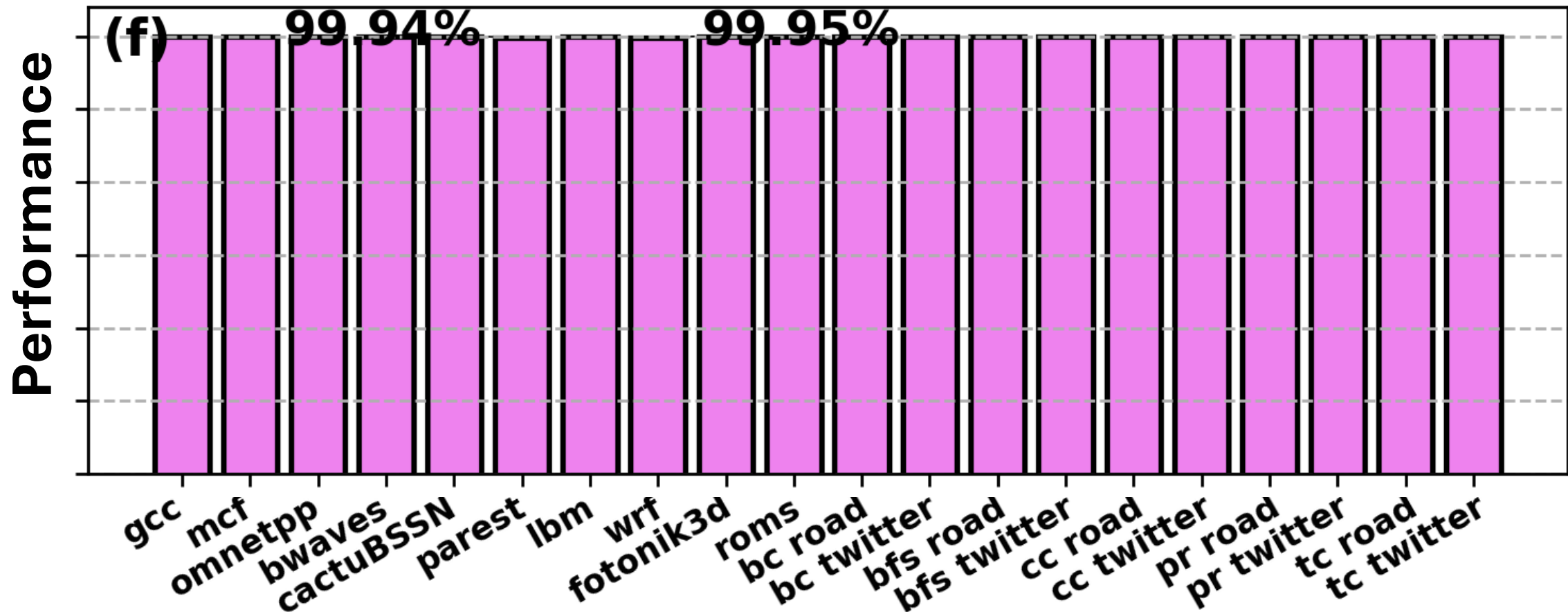
# Design1: SCREME-WO(Write-Only ECC)

Regular: 6400MHz & Slow: 3200MHz

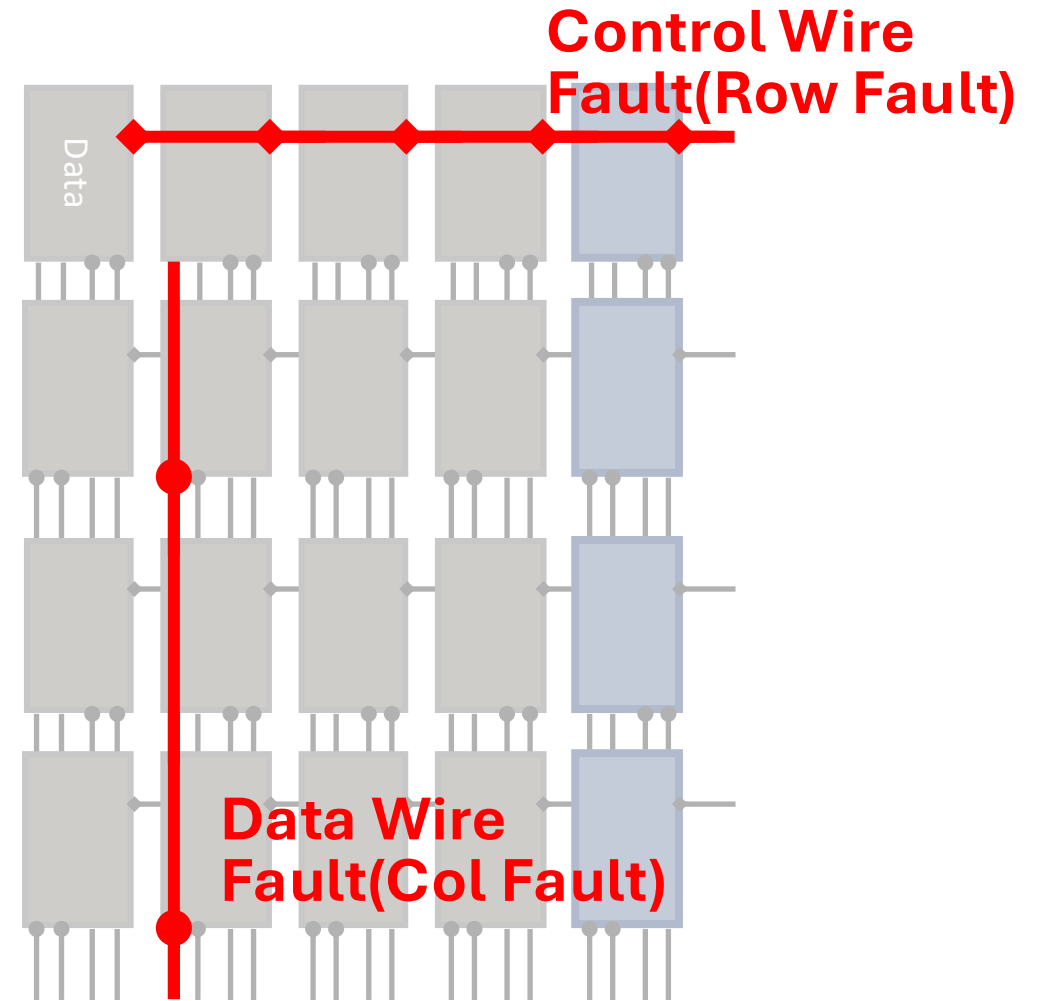
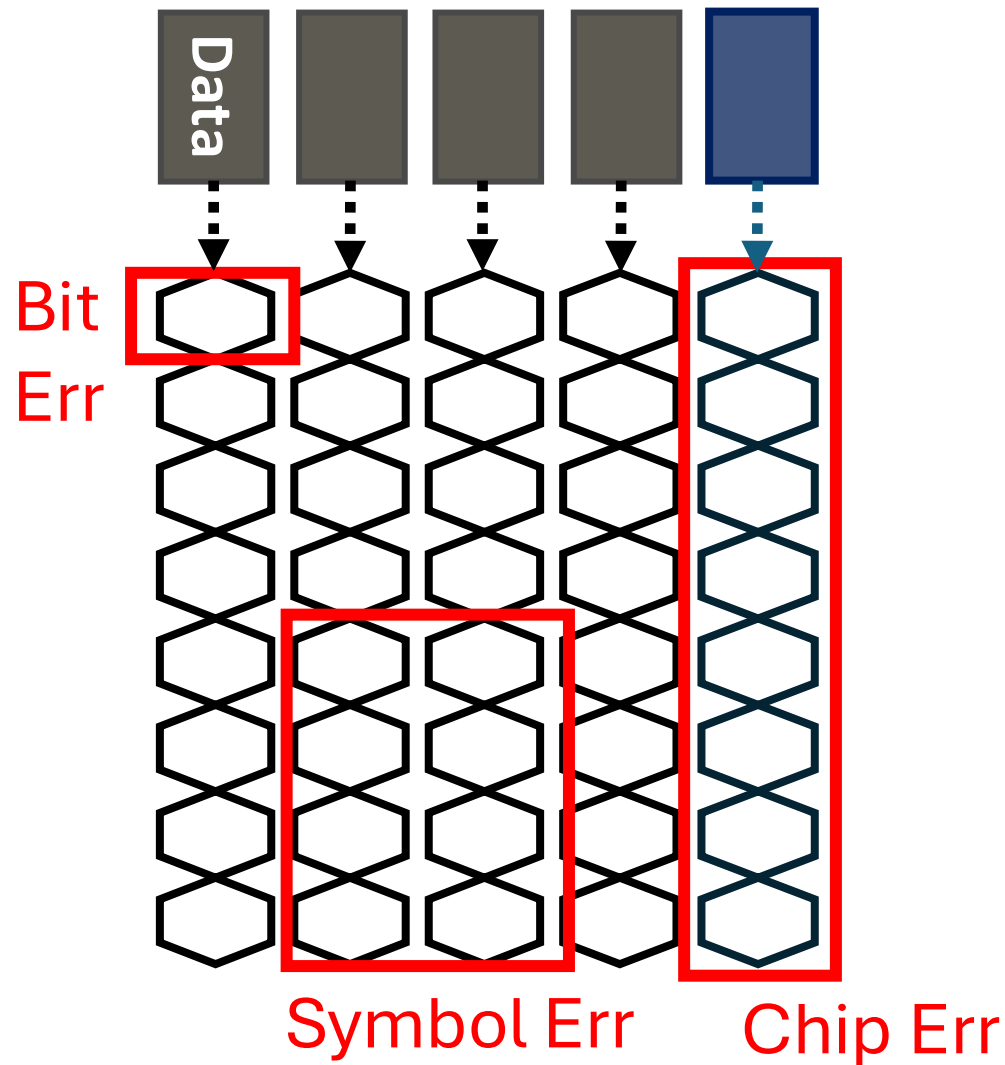


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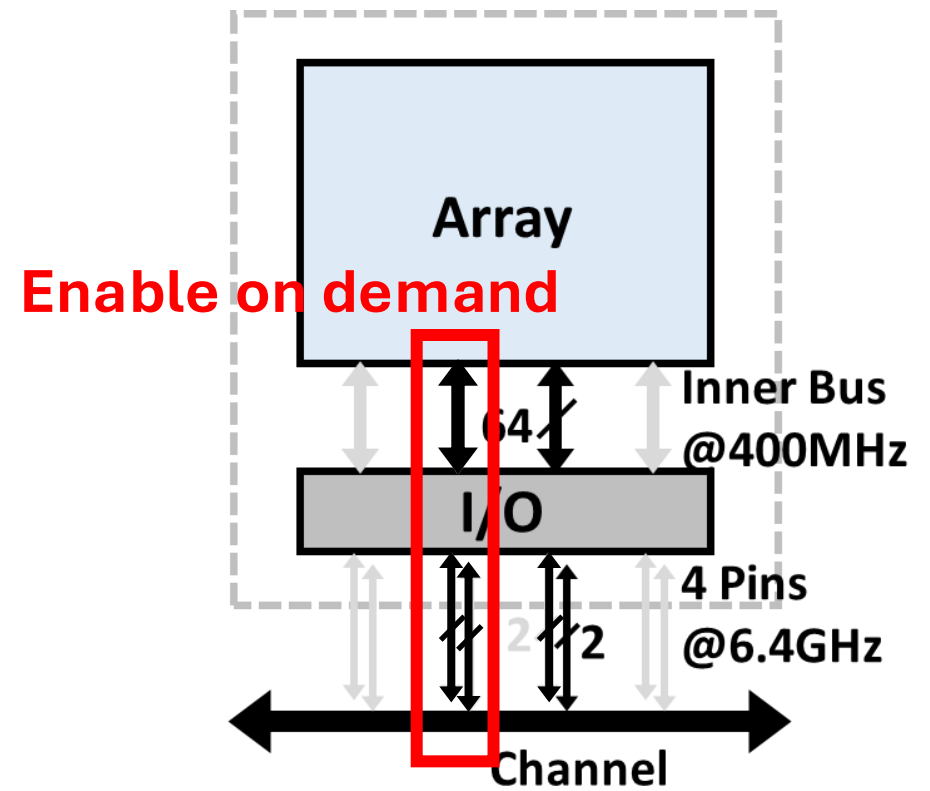
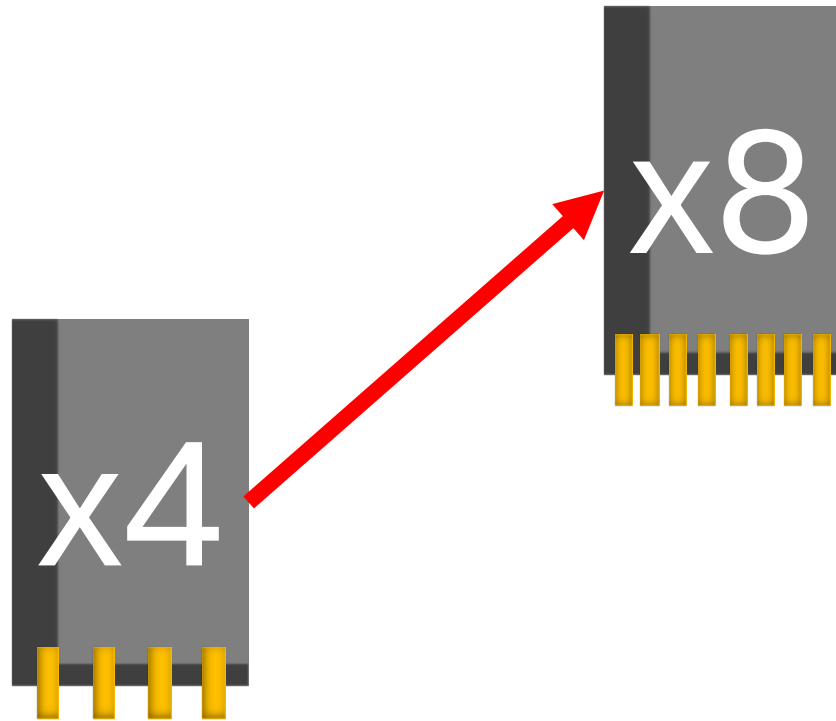
Regular: 6400MHz & Slow: 3200MHz



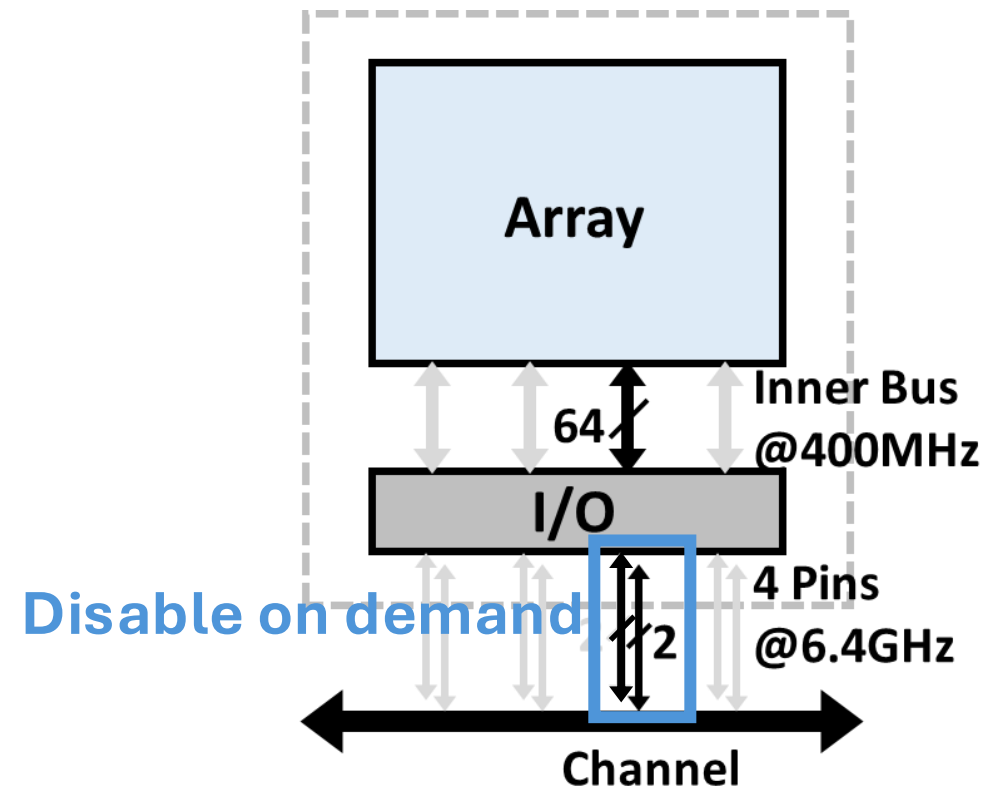
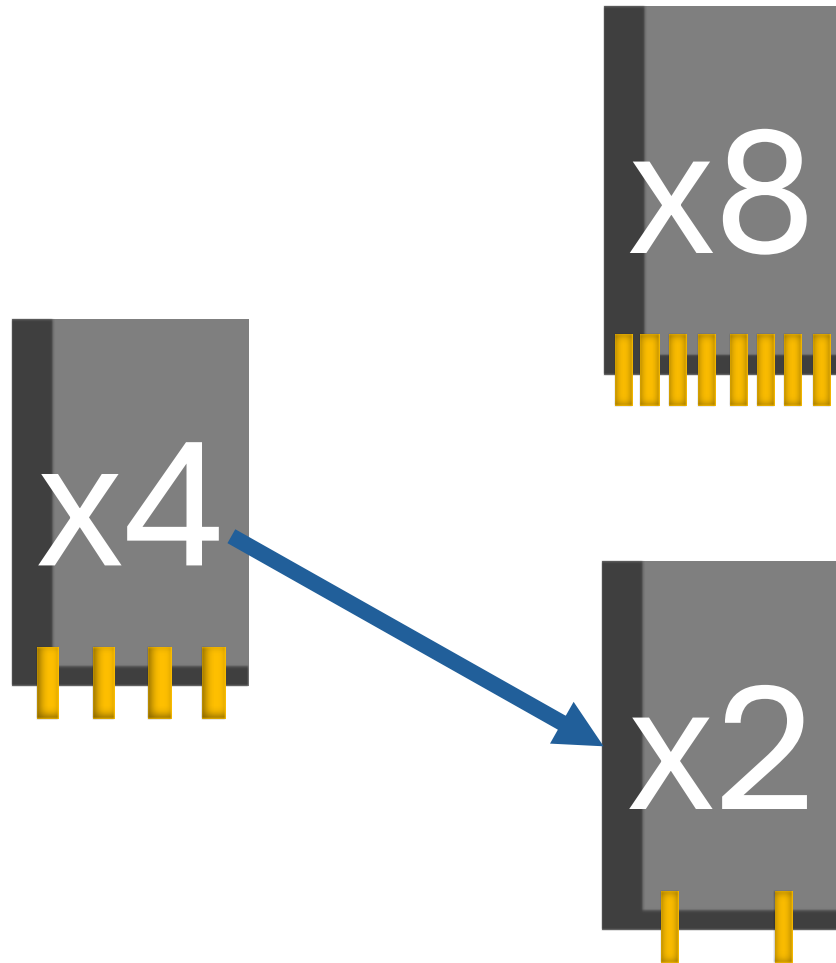
# Design2: SCREME-I/O



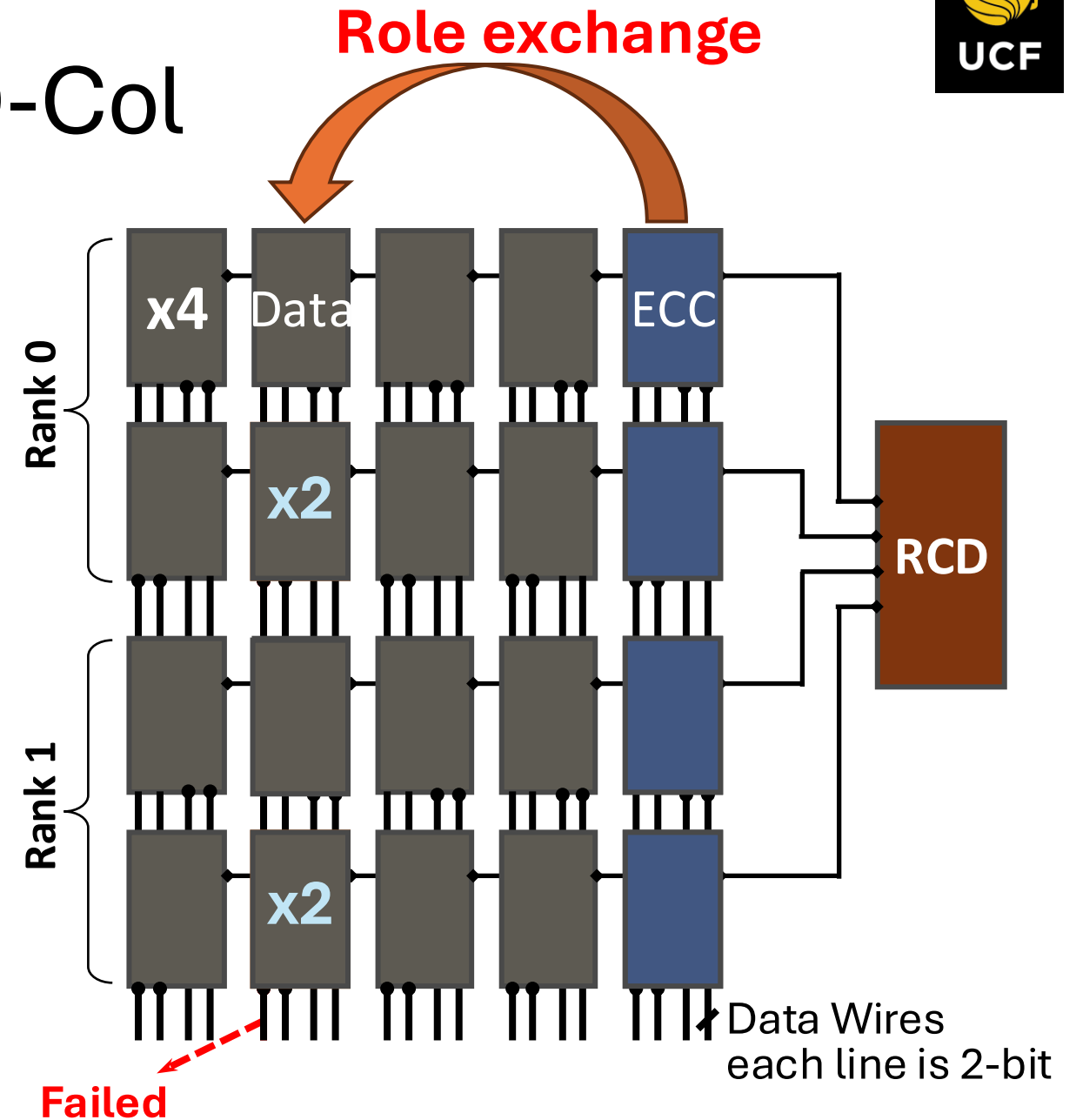
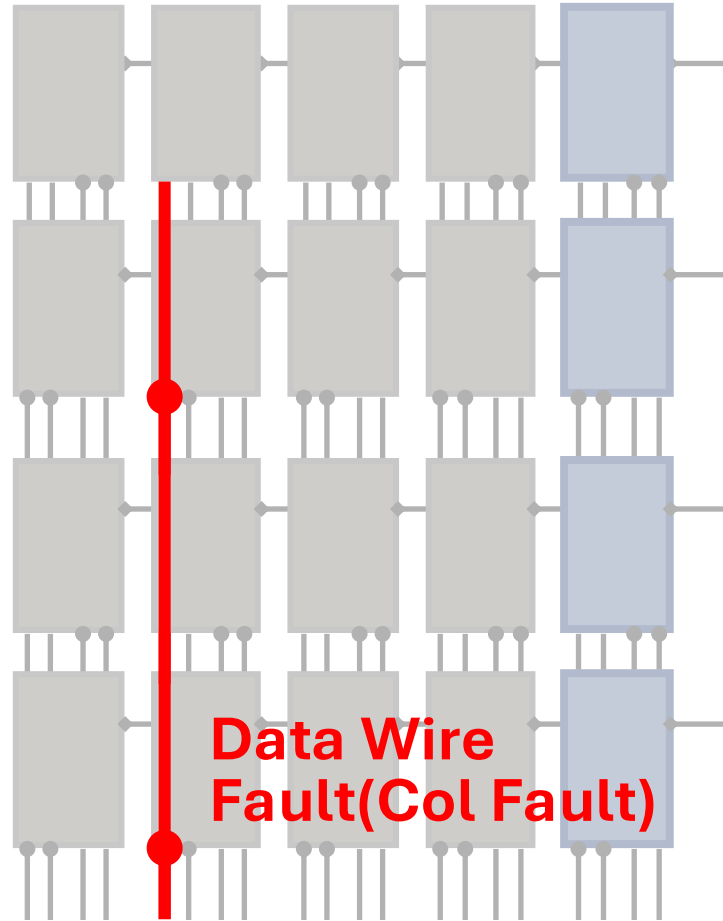
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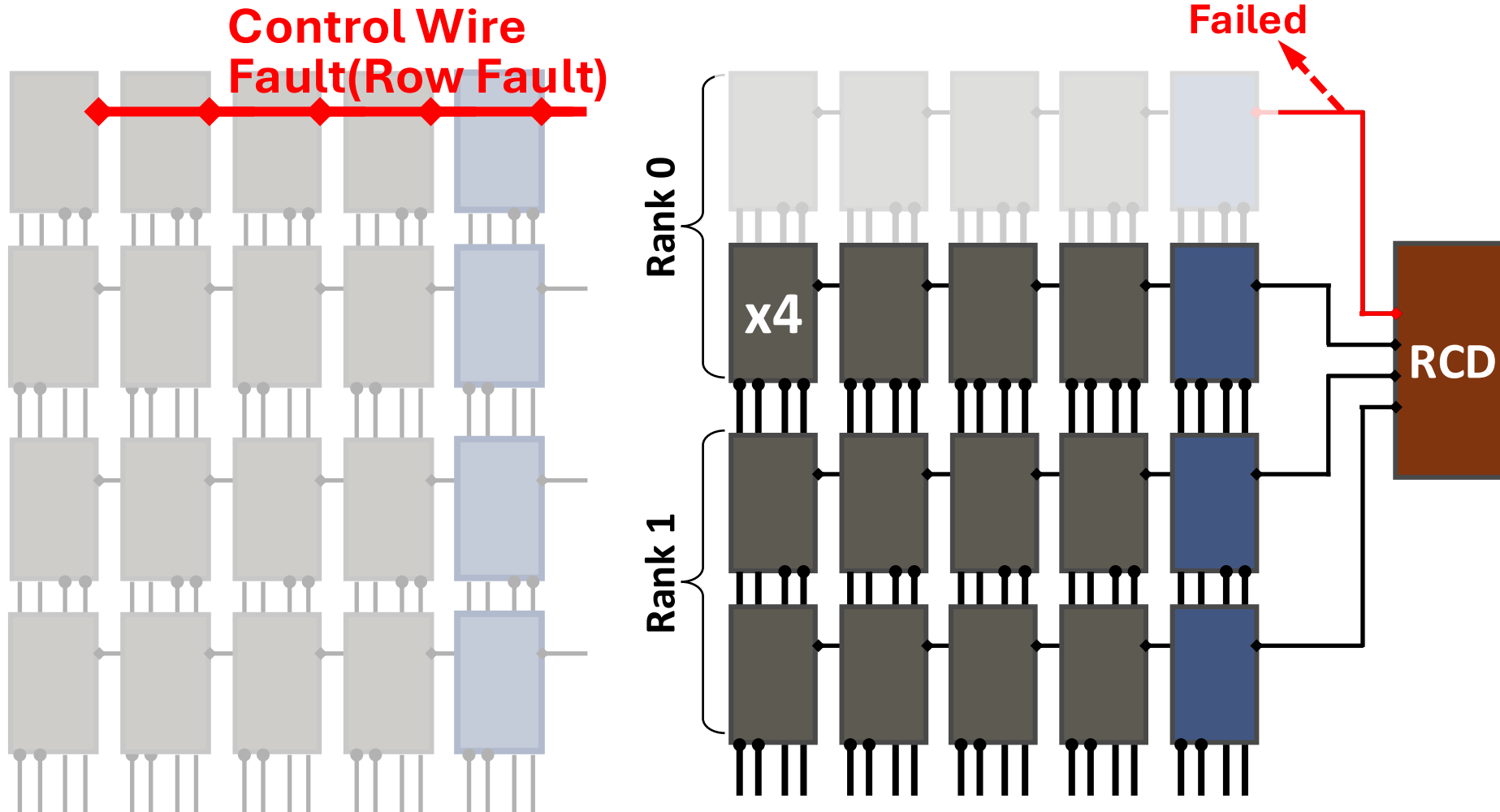
# Design2: SCREME-I/O



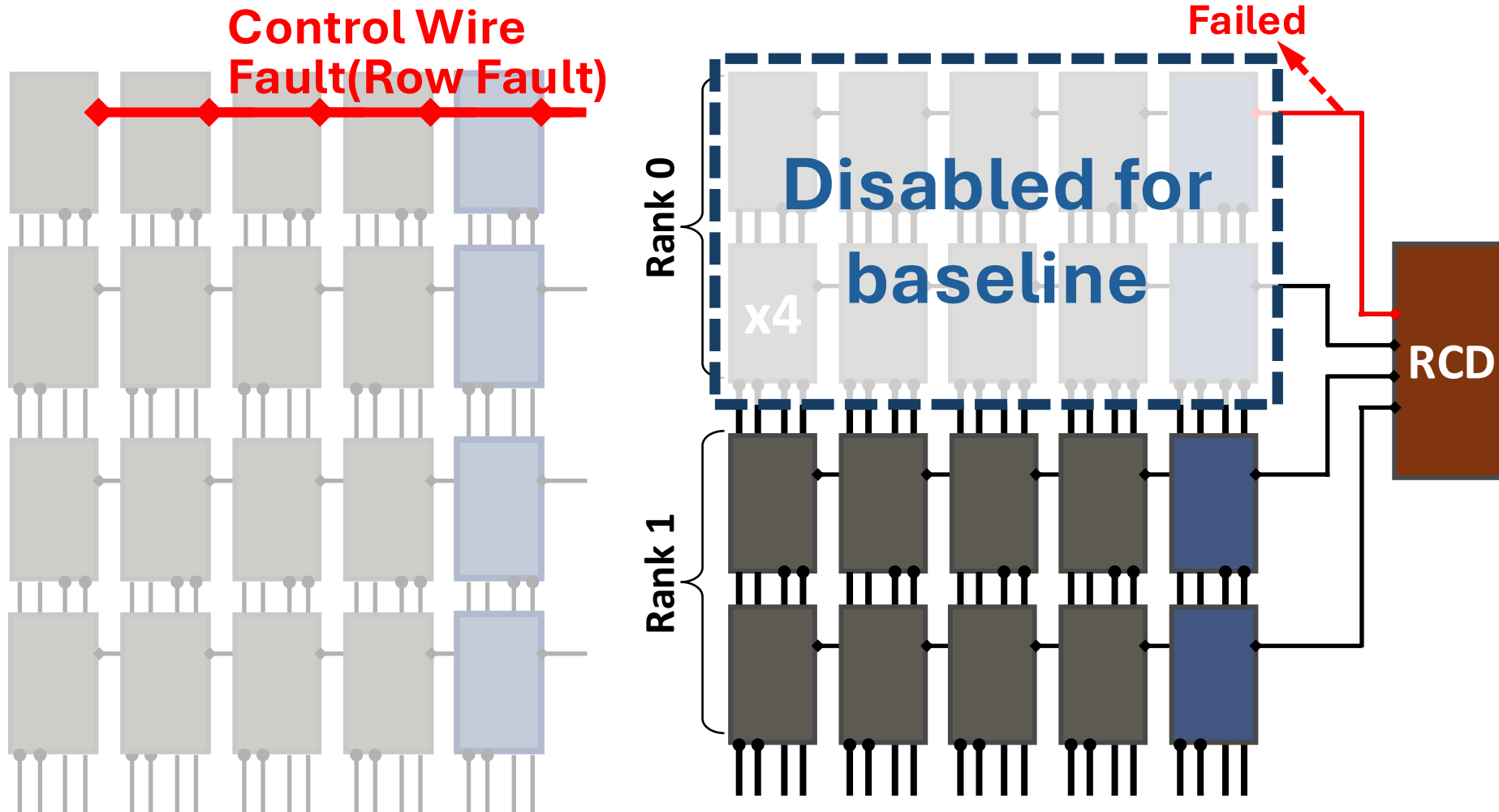
# Design2: SCREME-I/O-Col



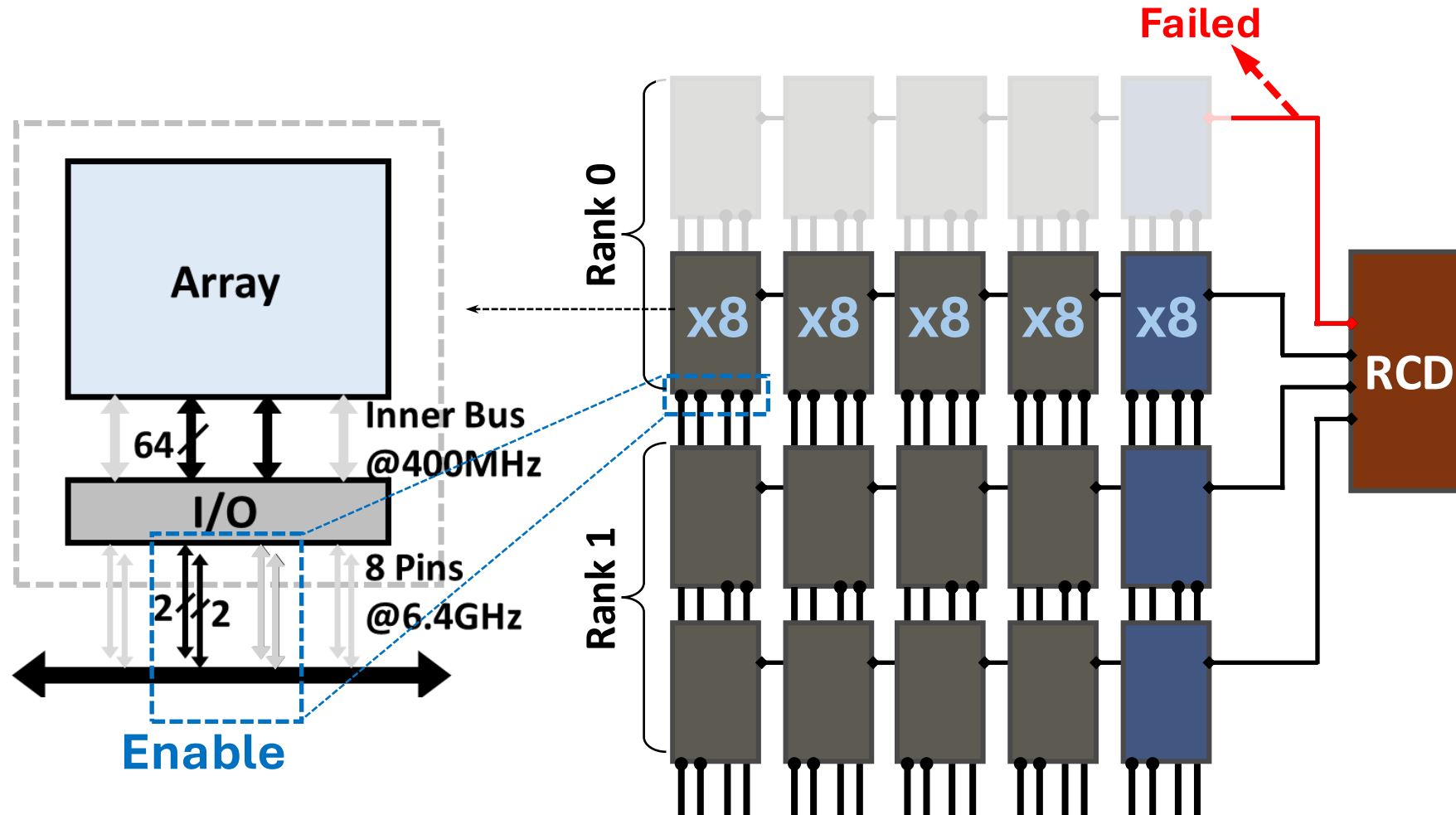
# Design2: SCREME-I/O-Row



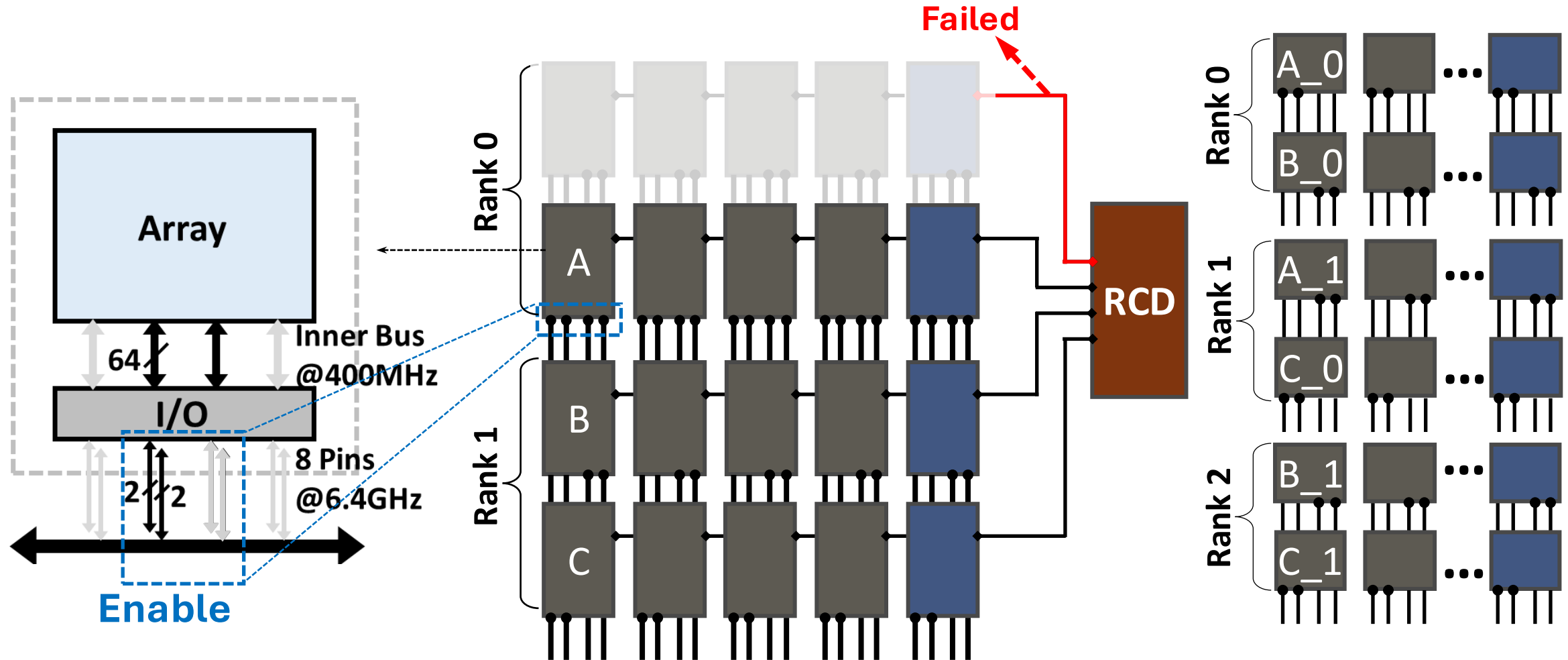
# Design2: SCREME-I/O-Row



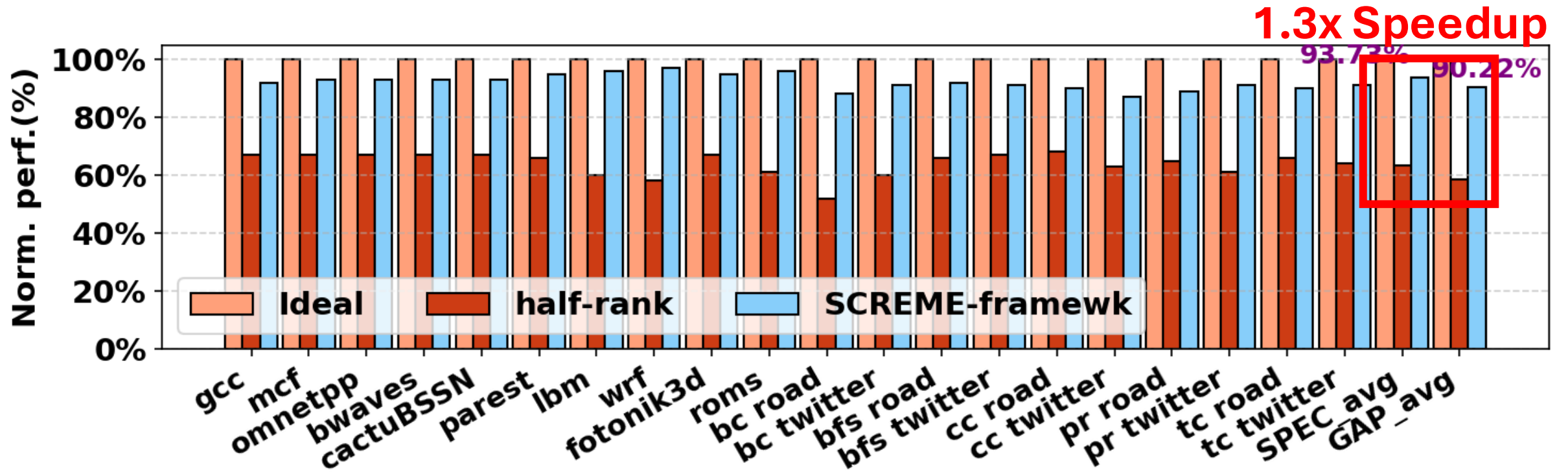
# Design2: SCREME-I/O-Row



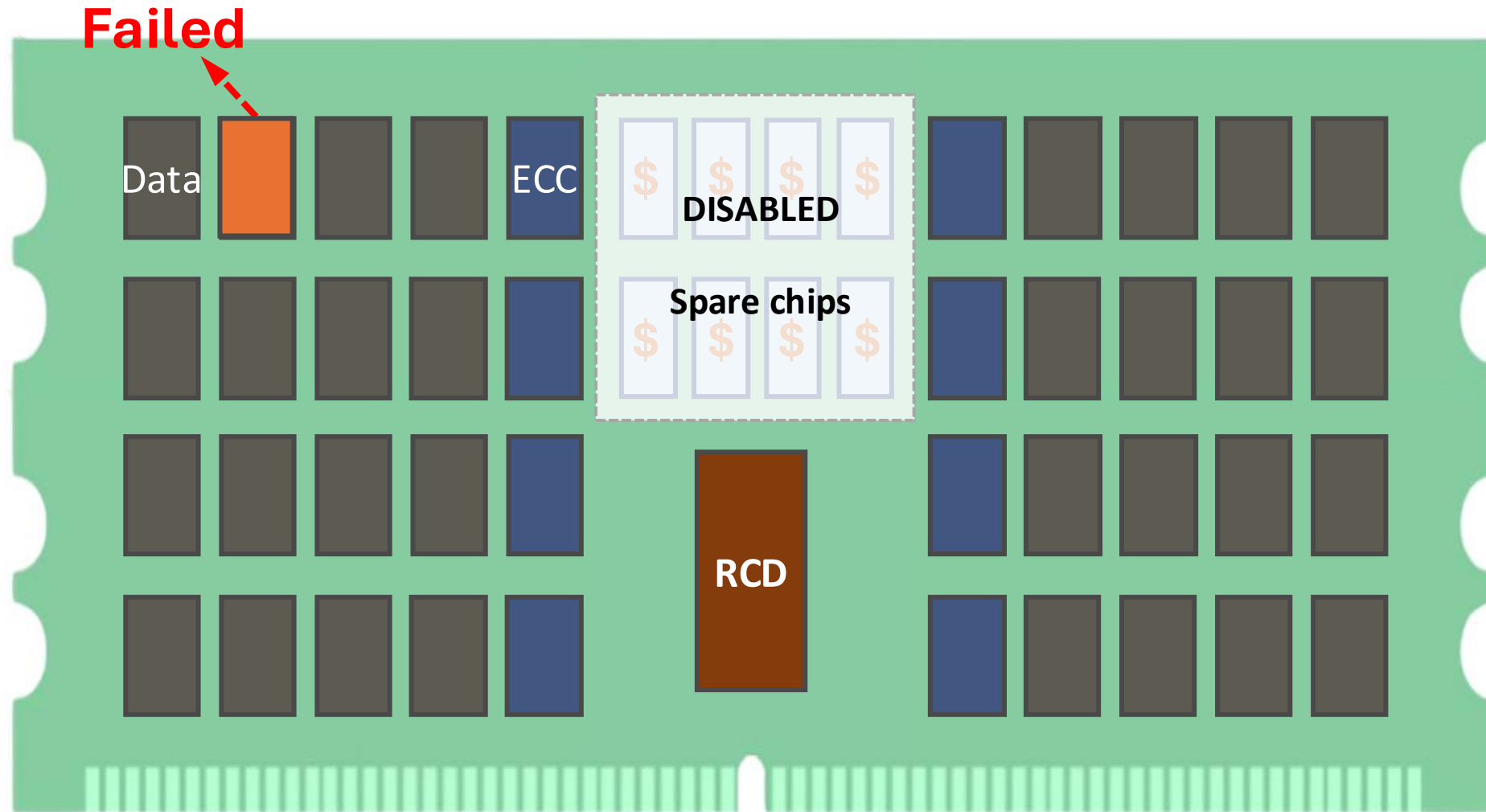
# Design2: SCREME-I/O-Row



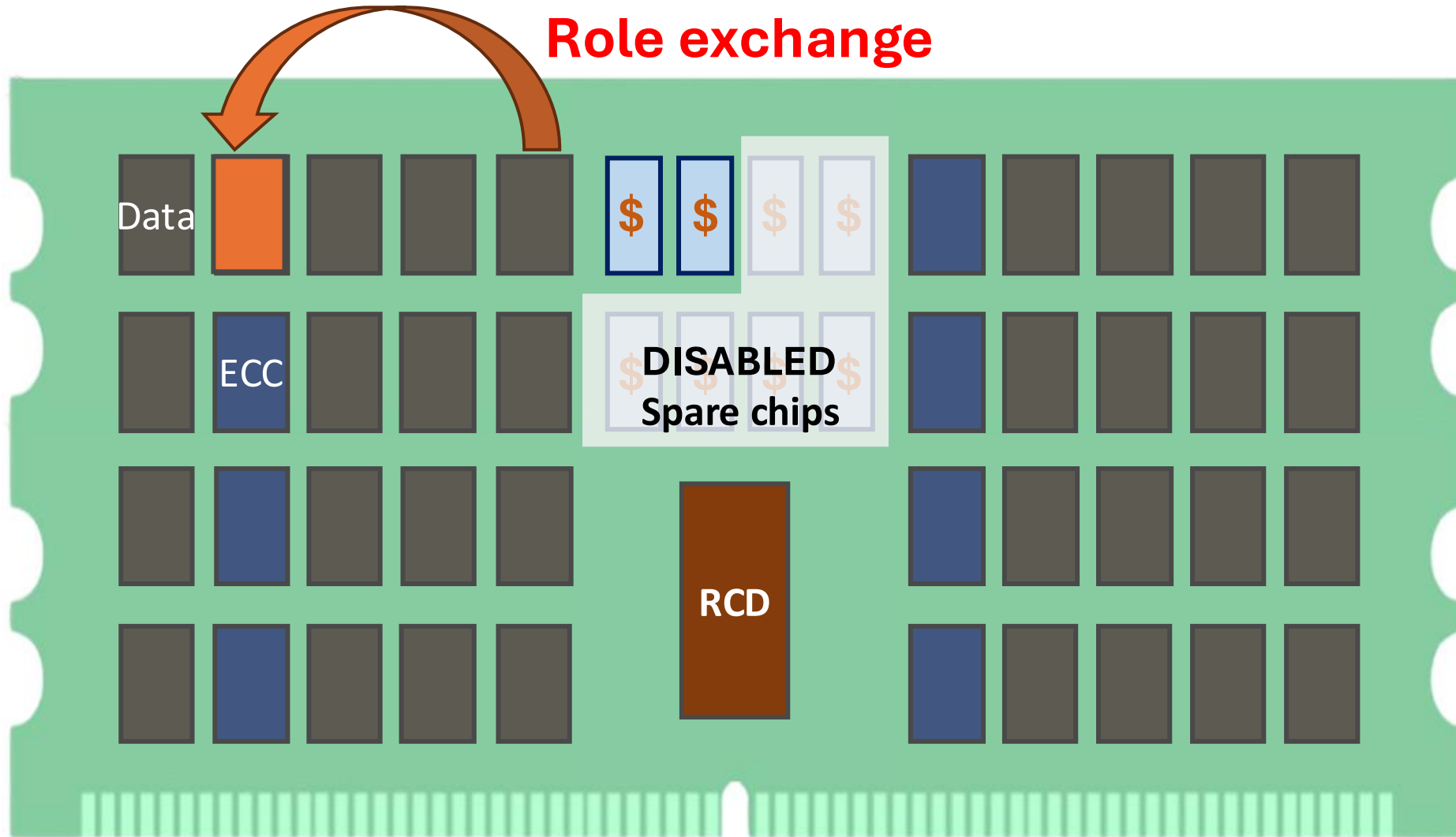
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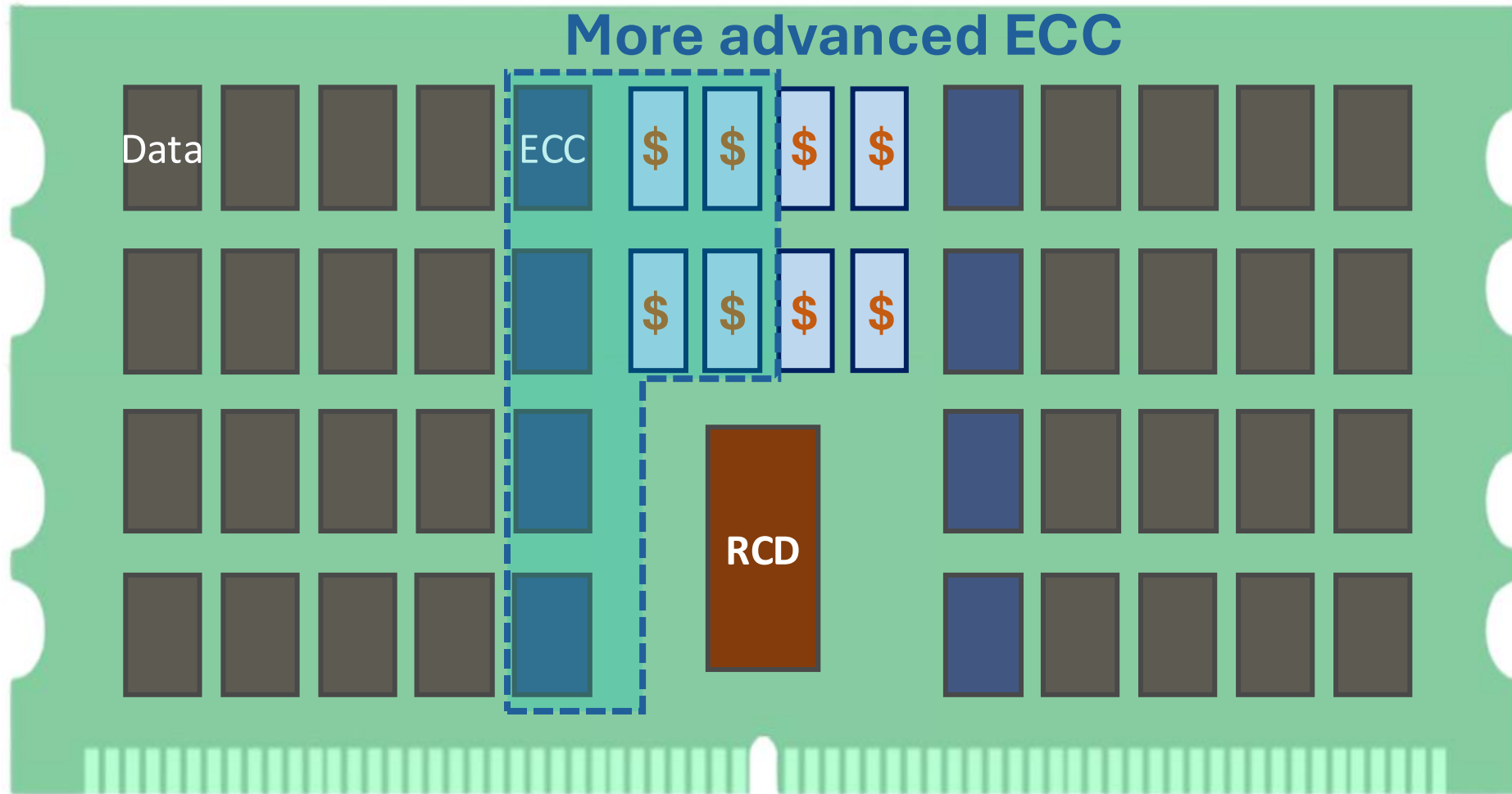
# Design3: SCREME-Framework



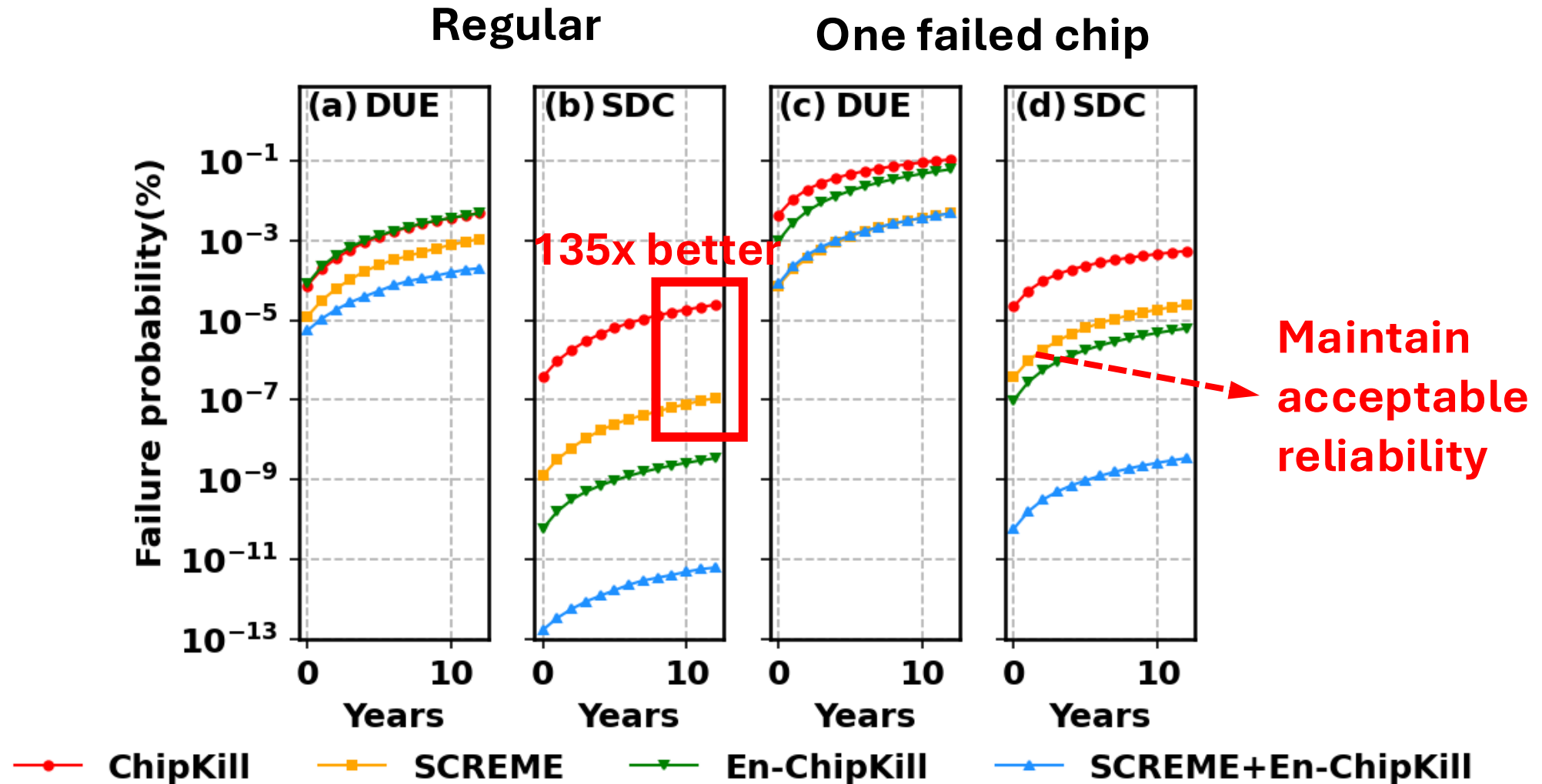
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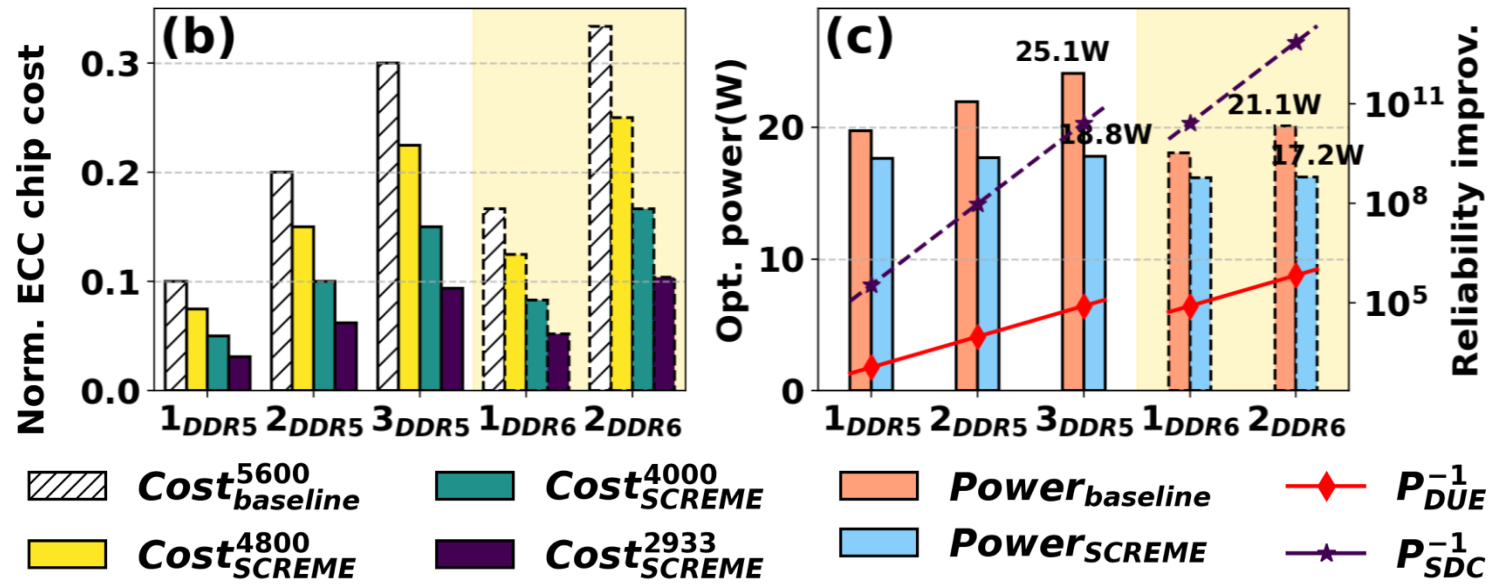


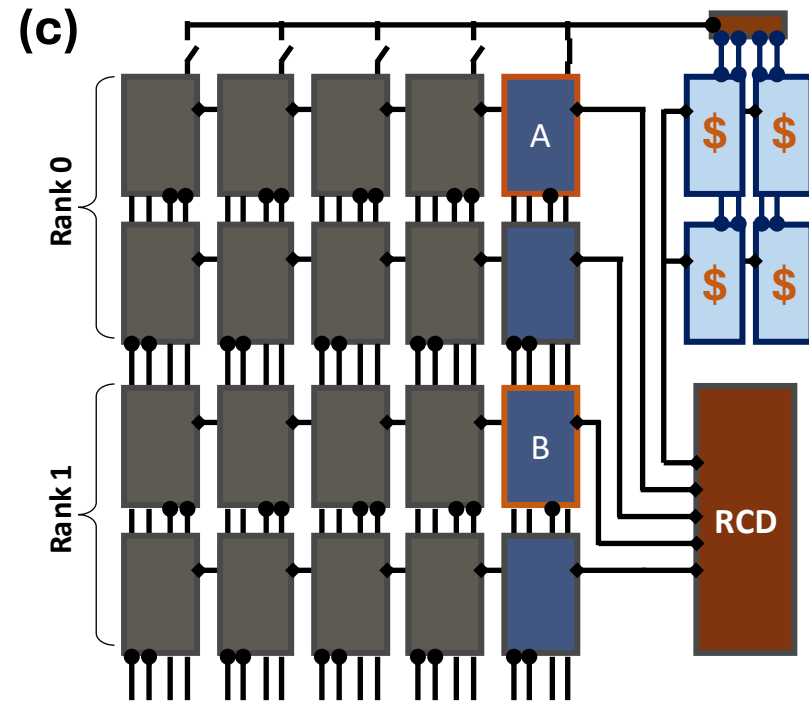
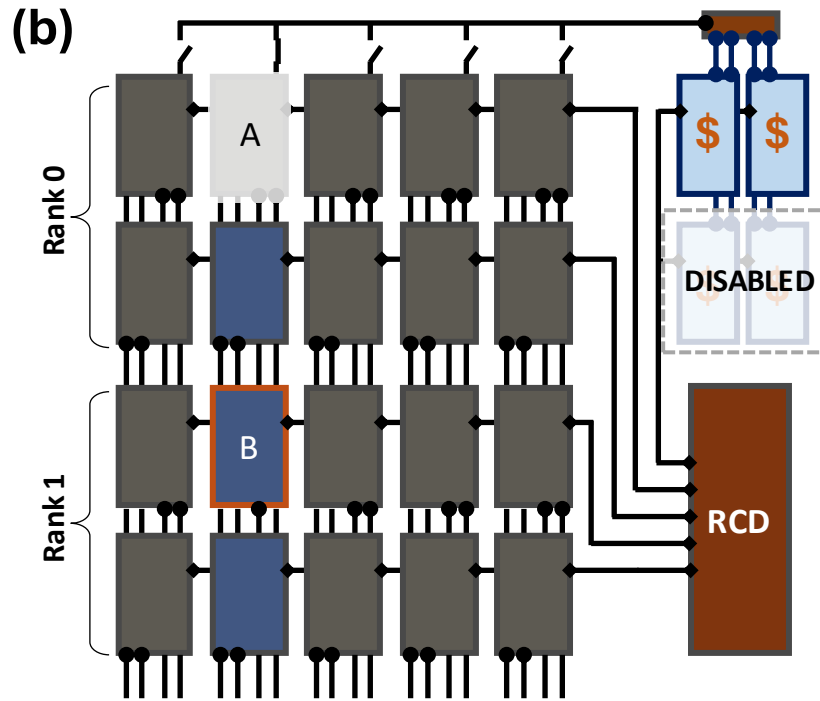


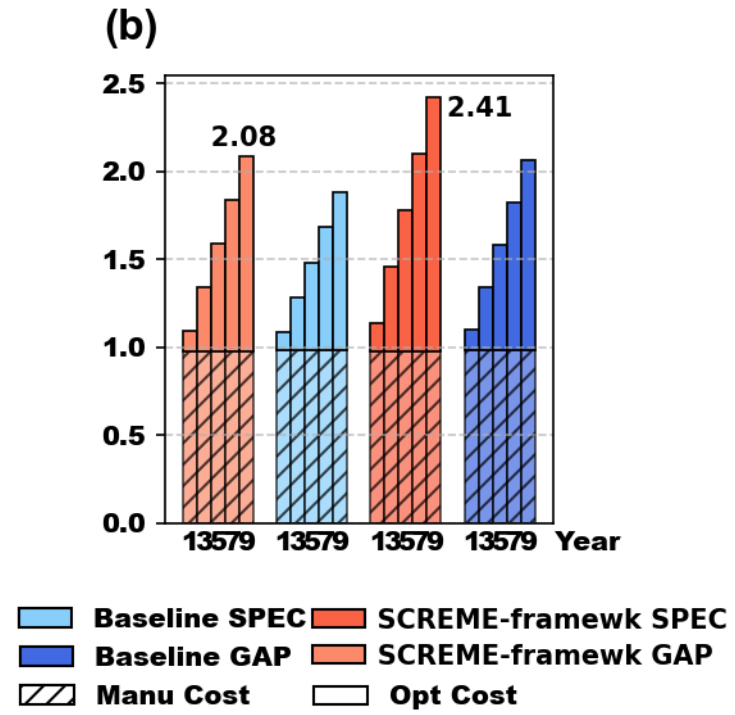
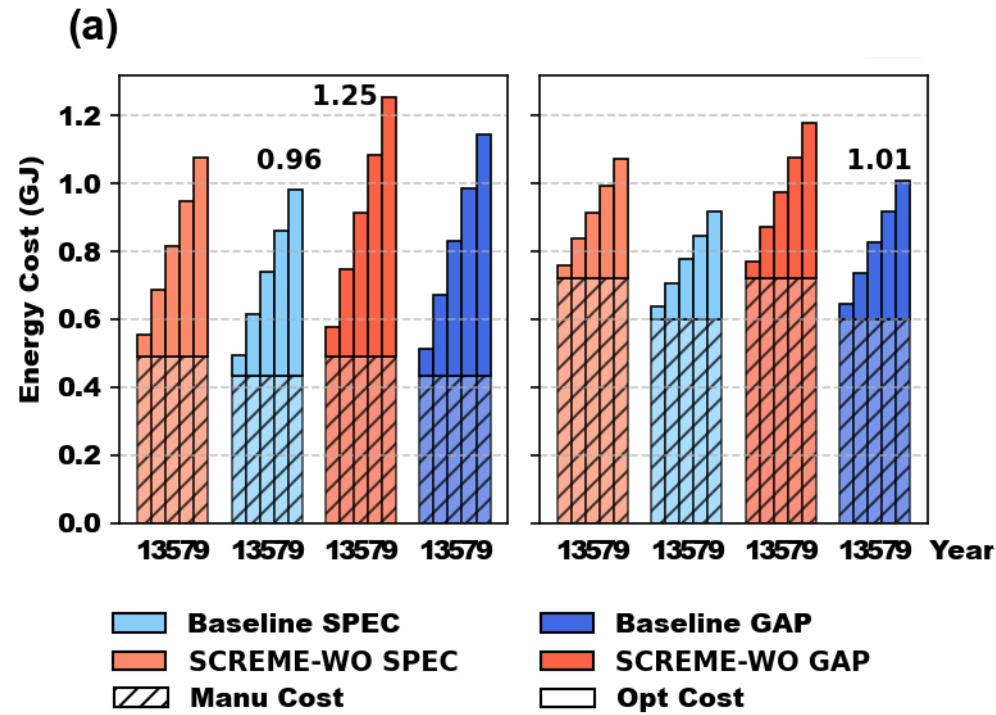
**Thank you for listening**

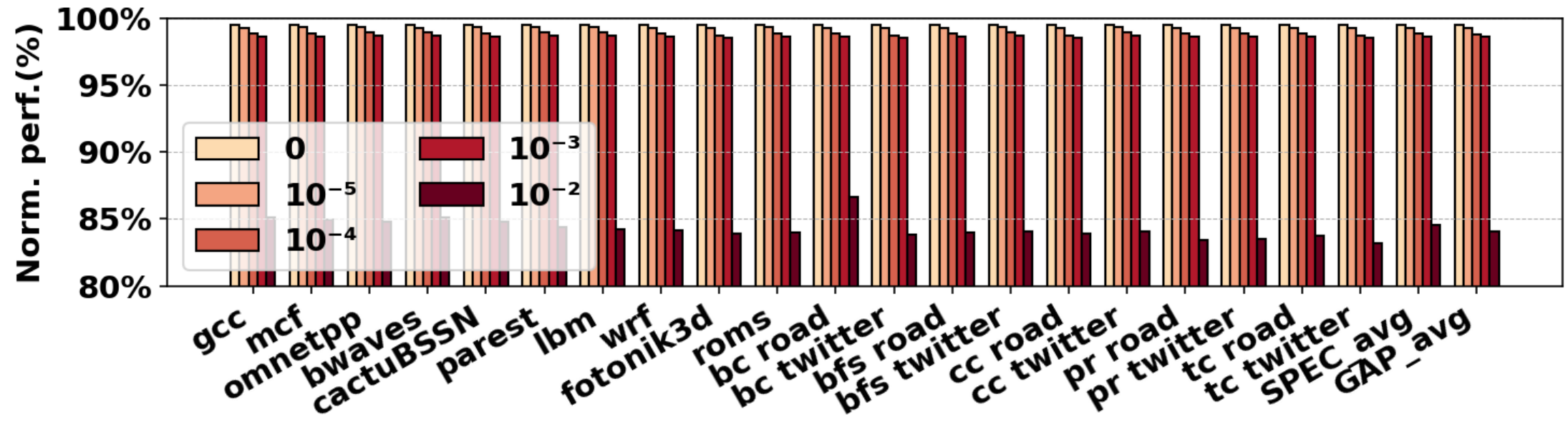
## SYSTEM CONFIGURATION AND BENCHMARKS

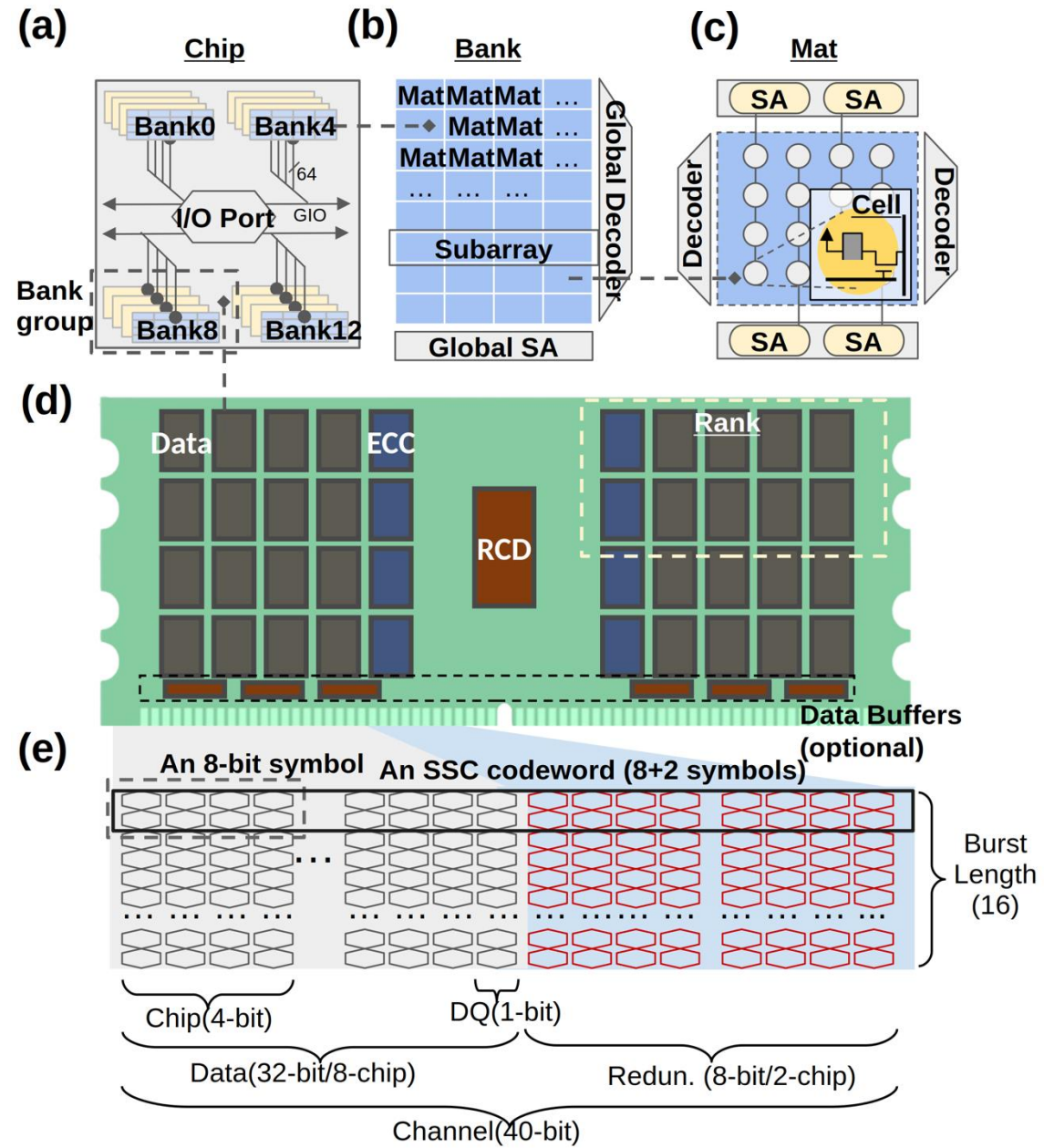
Processor	32 cores, 4.0GHz, non-inclusive L1: 16KB, 64B cacheline, 8-way asso. L2: 256KB, 64B cacheline, 8-way asso. LLC: 1MB/core, 64B cacheline, 16-way asso.
Memory Controller	Write queue capacity: 32 Page management: open-page Scheduler: FR-FCFS Data buffer latency: 4
DRAM Memory	DDR5-6400, 4GB, $\times 4$ I/O width 2 channels, 2 ranks, 8 banks-groups, 4 banks/bank-group 8Kb local row buffer CL-nRCD-nRP-nRAS: 44-44-44-81 nCCDS-nCCDL-nCCDLWR: 8-16-64
Benchmarks	<b>SPEC2017 CPU</b> <b>int:</b> gcc, mcf, omnetpp. <b>fp:</b> bwaves, cactuBSSN, parest, lbm, wrf, fotonik3d, roms <b>GAP</b> bc road, bc twitter, bfs road, bfs twitter, cc road, cc twitter, pr road, pr twitter, tc road, tc twitter











Fault Scenario	Decod. Result	ChipKill only	Decp. ChipKill		ChipKill w/ on-die ECC	Intel DDDC	SCREME Framwk
			Detect phase	Correct phase			
SBF(%)	DCE	100	-	100	100	100	100
SBF+	DCE	87.507	-	87.503	100	100	100
SBF(%)	DUE	12.101	99.951	12.108	0	0	0
	SDC	0.392	0.049	0.389	0	0	0
DBF(%)	DCE	100	-	100	100	100	100
	DUE	0	100	0	0	0	0
	SDC	0	0	0	0	0	0
SCF(%)	DCE	100	-	100	100	100	100
	DUE	0	100	0	0	0	0
	SDC	0	0	0	0	0	0